IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Inter Partes Review of: )
U.S. Patent No. 7,804,734 )
Issued: September 28, 2010 )
Application No.: 12/193,952 )
Filing Date: Aug. 19, 2008 )

For: Data Strobe Buffer and Memory System Including the Same

FILED VIA PRPS

PETITION FOR INTER PARTES REVIEW
OF U.S. PATENT NO. 7,804,734

For ease of reference, Petitioner refers to this Petition as “‘734 Petition #2,” challenging claims 1, 7–9, 12, 13, 17, and 19 of the ’734 patent. On April 17, 2015, Petition filed “‘734 Petition #1” challenging claims 1, 3, 7–9, 12, 13–15, 17, and 19 of the ’734 patent based on different prior art and grounds of invalidity.
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1102 File History for the ’734 patent
1103 U.S. Patent No. 6,819,602 (“Seo”)
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1107 Declaration of Dr. Bruce Jacob in support of Petition for Inter Partes Review of U.S. Patent No. 7,804,734 (“Jacob Decl.”)
1009 Samsung’s Second Amended Complaint in Civil Action No. 3:14-CV-00757-REP (E.D. Va.)
I. INTRODUCTION

On behalf of NVIDIA Corp. (“Petitioner”) and under 35 U.S.C. § 311 and 37 C.F.R. 42.100, inter partes review of claims 1, 7–9, 12, 13, 17, and 19 (“challenged claims”) of U.S. Patent No. 7,804,734 (“‘734 patent”), titled “Data Strobe Buffer and Memory System Including the Same,” is requested. According to PTO records, the ’734 patent was originally assigned to, and is currently owned by, Samsung Electronics Co., LTD. (“Patent Owner”). A copy of the ’734 patent is attached as Ex. 1101, and the prosecution history is attached as Ex. 1102.

A. This Petition Relies on Samsung’s Own Prior Art

The ’734 patent issued to Samsung in 2010. Yet six years earlier, Samsung was issued two other patents—U.S. Patent Nos. 6,819,602 (“Seo”) and 7,173,871 (“Kong”)—covering the same Samsung memory technology and features. Seo and Kong render the ’734 patent obvious, and they are the prior art references relied upon in this inter partes review petition.

The listed inventors of the three Samsung patents (the ’734 patent, Seo, and Kong) are all Samsung employees who worked at Samsung in Korea at the time these patents were filed. Seo and Kong are also contemporaries of each other. All three patents deal with Samsung memory technologies and features, solve the same memory problems, and it is likely that the Samsung engineers involved would have known of each other’s work. Certainly, the listed inventors to the Seo and Kong
patents qualify as persons of ordinary skill and would have presumptively known of each other’s work. And working at the same company and on the same technology would have further motivated them to incorporate each other’s work with their own to obtain design efficiency and reduce time to market. The ’734 patent merely arranges elements already disclosed by Seo and Kong. But “when a patent simply arranges old elements with each performing the same function it had been known to perform and yields no more than one would expect from such an arrangement, the combination is obvious.” *KSR*, 127 S. Ct., 1727, 1740 (2007).

B. No Redundancy or Duplication with ’734 Petition #1

On April 17, 2015, Petitioner filed a petition for *inter partes* review challenging the validity of certain claims of the ’734 patent (“’734 Petition #1”). This Petition (“’734 Petition #2”) also challenges the ’734 patent and is not redundant or duplicative for several reasons. As mentioned, this Petition focuses exclusively on Samsung’s own prior art and shows how Samsung’s ’734 patent is rendered obvious by its own prior art. In contrast, ’734 Petition #1 relies primarily on third-party prior art, U.S. Patent No. 7,032,092 (“Lai”). Lai is a patent developed and owned by VIA Technologies, Inc. of Taiwan.

This Petition #2 also challenges different claims and relies on different grounds of invalidity from Petition #1. This Petition is based on obviousness and shows that Seo in view of Kong render claims 1, 7–9, 12, 13, 17, and 19 obvious.
In contrast, ’734 Petition #1 is primarily based on anticipation, shows instead that Lai anticipates claims 1, 7–9, 12, 13, 17, and 19. Unlike Petition #1, this Petition does not challenge claims 3, 14, and 15.

The Seo prior art (from Samsung) relied on in this Petition is also different from the Lai prior art (from VIA Technologies) relied on in ’734 Petition #1. Seo is directed to a Multimode Data Buffer and Method for Controlling Prorogation Delay Time, and describes a data strobe buffer and delay circuit. Seo at Figure 7; 6:63–65 (showing delay circuit). In contrast, Lai is directed to a Memory Controller for Supporting a Plurality of Different Memory Access Modes, and describes a data strobe buffer and the memory controller containing the data strobe buffer. Lai at Figure 9; 3:47–48 (showing memory controller). Further, Lai, unlike Seo, explicitly discloses a driver circuit and buffer for generating data strobe signals Id. at Figure 9; 6:51–58. Because of these differences, this Petition relies on Seo in combination with Kong to render the ’734 claims obvious; whereas Petition #1 relies on Lai alone to anticipate the same ’734 claims obvious.

II. REQUIREMENTS FOR PETITION FOR INTER PARTES REVIEW

A. Grounds for Standing (37 C.F.R. § 42.104(a))

Petitioner certifies that the ’734 patent is available for inter partes review and that Petitioner is not barred or estopped from requesting inter partes review of the challenged claims of the ’734 patent on the grounds below.

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B. Notice of Lead and Backup Counsel and Service Information

Under 37 C.F.R. §§ 42.8(b)(3), 42.8(b)(4), and 42.10(a), Petitioner provides the following designation of Lead and Back-Up counsel.

<table>
<thead>
<tr>
<th>LEAD COUNSEL</th>
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Under 37 C.F.R. § 42.10(b), a Power of Attorney is attached.

C. Notice of Real-Parties-in-Interest (37 C.F.R. § 42.8(b)(1))

The real-party-in-interest is NVIDIA Corporation. No other party exercised or could have exercised control over this petition; no other party funded or directed this petition. (See Office Patent Trial Practice Guide, 77 Fed. Reg. 48759–60.)

D. Notice of Related Matters (37 C.F.R. § 42.8(b)(2))

_Certain Graphics Processing Chips, Systems on a Chip, and Products Containing the Same_, 337-TA-941 (USITC). Petition for _inter partes_ review of
Petition for Inter Partes Review of USP 7,804,734

U.S. Patent No. 6,147,385 (IPR2015-01065). Petition for inter partes review of
U.S. Patent No. 7,056,776 (IPR2015-01062). Petition for inter partes review of
no applications claim the benefit of the priority of the filing date of the ’734 patent.

E. Fee for Inter Partes Review

The Director is authorized to charge the fee specified by 37 CFR § 42.15(a)
to Deposit Account No. 506269.

F. Proof of Service

Proof of service of this Petition on the Patent Owner at the correspondence
address of record for the ’734 patent is attached.

III. IDENTIFICATION OF CLAIMS BEING CHALLENGED
(§ 42.104(B))

Claims 1, 7–9, 12, 13, 17, and 19 of the ’734 patent (the “challenged
claims”) are unpatentable in view of the following prior art:

• U.S. Patent No. 6,819,602 (“Seo,” attached as Ex. 1103)
• U.S. Patent No. 7,173,871 (“Kong,” attached as Ex. 1104)

Specifically, the challenged claims are invalid under 35 U.S.C. § 103 because they
are rendered obvious by Seo in view of Kong.

IV. DESCRIPTION OF PURPORTED INVENTION

The ’734 patent is entitled “Data Strobe Buffer and Memory System
Including the Same.” It relates generally to memory devices and specifically to
A. Technology Background

The ’734 patent relates to communication between devices in a computer and the computer’s main memory. *Id.* at ¶ 28–29. A computer communicates with DRAM memory using a circuit called a memory controller, see *id.* at ¶¶ 30–32:

![Diagram of memory controller and DRAM memory device]

The box on the left is a memory controller—the circuit that a microprocessor uses to communicate with the memory device. *Jacob Decl.* at ¶ 33. The box on the right is a semiconductor memory device such as DRAM memory. *Id.* The lines labeled “DQS” and “DQ” are wires used to transmit electrical signals between the memory controller and the memory device. See *id.*; see also ’734 patent at 3:48–56.

The memory controller sends and receives data to and from a memory device. *Jacob Decl.* at ¶ 34. In annotated Figure 1 of the ’734 patent below, the line or wire “DQ” (highlighted in blue below) is the transmission path for data signals between the memory controller and the memory device. *Id.* at ¶ 35. The arrows on both sides of the DQ line indicate that it is bi-directional: the memory controller...
might transmit a data signal on a line during a write operation, but receive a data signal on the same line during a read operation. *Id.* at ¶ 36. A data signal is an electrical signal that represents the underlying data sequence, *id.* at ¶ 37:

![Diagram of data transmission](image)

The memory controller reconstructs the original data sequence of the data signal by using another signal—a *data strobe signal*—as a timing reference, *id.* at ¶¶ 38–40:

![Diagram of data strobe](image)

The orange signal is a data strobe signal. *Id.* at ¶ 41. It is a periodic signal that changes between high and low voltage on a regular cycle while the data is being
transmitted. *Id.* The memory controller uses the transitions or “edges” of the data strobe signal to determine when to measure the value of the data signal. *Id.*

Memory devices and controllers may have to amplify the data strobe signal before it can be used as a timing reference. *Id.* at ¶ 42. The following figure illustrates the data and data strobe signals being transmitted at a low amplitude but then amplified into a higher amplitude signal after arriving at the controller:

The component of a memory device or controller that processes the received data strobe signal is called a “data strobe buffer.” *Id.* ¶ 43. It is called a “buffer” because it acts as an intermediary: it receives the data strobe signal from the bus and outputs the internal data strobe signal for the receiving chip. *Id.* It is also
responsible for driving a data strobe signal during a write operation. *Id.* The ’734 patent is directed to “data strobe buffers,” and in particular, how the received data strobe signal is amplified (if at all) to produce the internal signal. *Id.*

The ’734 patent describes two different signaling schemes for transmitting the data strobe signals: “single-ended” and “differential.” ’734 patent at 1:33–36; Jacob Decl. at ¶ 44. Single-ended signals use a *single physical wire* to send a single logical signal. Jacob Decl. at ¶ 45. Differential signals use a *pair of physical wires* to send a single logical signal via two physical signals: the primary (or “true”) signal and its inverse. Each scheme also uses different amplification process. *Id.*

To amplify a single-ended data strobe, a memory controller uses a circuit such as a comparator. *Id.* at ¶ 46. The received data strobe signal is input into the comparator along with a flat voltage called a reference voltage. *Id.* The comparator tests the data strobe signal to see if it is above or below the reference voltage, and, depending on the result, amplifies the signal to be higher or lower. *Id.* at ¶¶ 46–47.

The mechanism is slightly different in a differential signaling system. Just as a single-ended scheme, the data strobe signal is amplified by performing a comparison. *Id.* at ¶ 48. But rather than comparing the data strobe signal to a reference voltage, it compares it to the inverse data strobe signal. *Id.* In a single-ended and differential signaling scheme, the comparator outputs an amplified signal with the same timing information as the original signal. *Id.* at ¶ 49–50.
B. Disclosure of the ’734 Patent

The ’734 patent relates to semiconductor memory devices generally, and more specifically, to a data strobe buffer that can be interfaced to different types of semiconductor memory devices, and a memory system including the data strobe buffer. ’734 patent at Abstract, Field of the Invention, 1:15–20. To address the problem of interfacing with different types of memory devices, the ’734 patent discloses a data strobe buffer with the ability to use either single-ended (such as for DDR memory) or differential data strobes (such as for DDR2 memory). Jacob Decl. at ¶¶ 51–54. The signaling scheme used will depend on the type of memory attached to the memory controller. Id.; see also ’734 patent at Summary of the Invention, 1:46–51. This allows a controller to interface with different memory devices, each of which may require a different data-strobe signaling scheme. Id.

As illustrated in Figure 4 of the ’734 patent, elements of the disclosed data strobe buffer can be divided into three classifications: (1) input/output node functionality, (2) driver functionality, and (3) receiver functionality. Jacob Decl. at ¶¶ 55–56. All of these elements (input/output nodes, drivers, and receivers) were well known in the art at the time of the purported invention. Id. at ¶¶ 56. The ’734 patent claims input/output node functionality (highlighted in blue) and memory controllers comprising either one or two input/output nodes. Id. at ¶¶ 57–58.
The input/output nodes are the gateways through which data strobe signals are sent to, or received from, the memory. *Id.* at ¶ 58. The ’734 patent also claims driver functionality (highlighted in green), in which a driver is used to drive a data strobe signal to the memory device during a write operation. *Id.* at ¶¶ 59–60.

The ’734 patent also claims receiver functionality (highlighted in orange), where a receiver receives a data strobe signal, processes it, and outputs the result. *Id.* at ¶¶ 61–62. The receiver can function in two different modes, and will process the data strobe signal differently depending on which mode is active. ’734 patent at 1:65–2:5. In some embodiments, the ’734 patent discloses a receiver that allows the data strobe buffer to use either single-ended or differential data strobos, which depends on the type of memory attached. *Id.* at 1:46–51; Jacob Decl. at ¶¶ 61–62.

In single-ended memory, the data strobe signal is compared to a reference
voltage (represented by the input T1 connected to Vref), whereas in differential memory, the data strobe signal is compared to its inverse (represented the input T2 which is connected to DQSB_2, a data strobe bar signal). *Id.* at ¶ 63. The ’734 patent claims a selector for “selecting” between the reference voltage and the data strobe bar signal. *Id.* at ¶ 64. In Figure 8A, the selector is shown as a multiplexer. *Id.* As shown below, the two “modes” of the patent are accomplished when the selector “selects” one of two signals to compare to the received data strobe signal:

![FIG 8A](image)

’734 patent at Figure 8A; *see also* Jacob Decl. at ¶¶ 63–67.
V. CLAIM CONSTRUCTION

Petitioner reserves all rights regarding 35 U.S.C. § 112. All claim terms not specifically addressed in this section have been accorded their broadest reasonable interpretation as understood by a person of ordinary skill and are consistent with the specification of the ’734 patent. Jacob Decl. ¶¶ 107–08. Petitioner submits that the following terms may need to be construed in connection with this IPR:

1. “coupled”

The term “coupled” is used in challenged claims 1, 7, 8, 12, 17 and 19. The specification states that “when an element is referred to as being ‘connected’ or ‘coupled’ to another element, it can be directly connected or coupled to the other element or intervening elements may be present.” ’734 patent at 2:57–60. Thus, the broadest reasonable interpretation of “coupled” is “connected either directly or through intervening elements.” See Jacob Decl. at ¶¶ 109–111.

2. “data strobe signal”

The term “data strobe signal” is used in challenged claims 1, 7, 12, 13, and 17. The specification does not define “data strobe signal.” A data strobe signal is a signal used to time data. Thus, the broadest reasonable construction of “data strobe signal” is a “signal used to time data.” Jacob Decl. at ¶¶ 112–114.

3. “data strobe bar signal”

The term “data strobe bar signal” is used in challenged claims 12 and 13.
The specification states: “The data strobe bar signal DQSB is an inverted signal of the data strobe signal DQS.” ’734 patent at 6:25–26. Thus, the broadest reasonable construction of “data strobe bar signal” is an “inverted data strobe signal.” Jacob Decl. at ¶¶ 115–117.

4. “input/output node”

The term “input/output node” is used in challenged claims 1, 7, 12, 13, and 17. The specification states: [t]he memory controller 100 interfaces with the memory device 200 through first through fourth input/output (I/O) pads P1 through P4.” ’734 patent at 3:44–48. The claims further make clear that the input/output node is a point in the circuit where signals may be input and output. Jacob Decl. at ¶ 118. Samsung’s proposed construction for “input/output node” in the related ITC matter, Inv. No. 337-TA-941, where the claim construction standard is plain and ordinary meaning, is “a point in a circuit through which signals may be input and output.” Samsung’s Preliminary Proposed Constructions at 9; Jacob Decl. at ¶ 119. The broadest reasonable interpretation of “input/output node” will be at least as broad as Samsung’s proposed construction. Id. Thus, the broadest reasonable construction of “input/output node” is “a point in a circuit through which signals may be input and/or output.” Jacob Decl. at ¶¶ 118–120.

VI. PERSON HAVING ORDINARY SKILL IN THE ART

For purposes of this review, a person of ordinary skill is a person with an
undergraduate degree in electrical engineering (or equivalent subject) with either:

(1) three to four years of post-graduate experience designing computer
memory systems, including one to two years of experience with double
date rate DRAM memory systems; or

(2) a master’s degree in electrical engineering (or an equivalent subject)
together with one to two years of post-graduate experience in designing
computer memory systems, including DDR DRAM systems.

Jacob Decl. at ¶¶ 25–57. A person of ordinary skill in the art would have also been
familiar with double data rate memory standards. Id. This description is
approximate, and a higher level of education or skill might make up for less
experience, and vice-versa. Id.

 VII. OVERVIEW OF THE PRIOR ART

For the Board’s ease of reviewing the prior art references, the declarant, Dr.
Jacob, has provided a glossary mapping terms in the ’734 patent to corresponding
terms used by the prior art references discussed herein. See Jacob Decl. at ¶ 94.

A. U.S. Patent 6,819,602 (“Seo”)

U.S. Patent 6,819,602 (“Seo,” attached as Ex. 1103) was filed on October
23, 2002 and claims priority to U.S. Provisional Patent App. No. 60/379,665, filed
May 10, 2002. Seo issued on November 16, 2004 and lists Samsung Electronics
Co., Ltd., of Korea as the assignee. Seo lists Seong-young Seo, Jung-bae Lee, and
Yong-mo Moon as the inventors, who were all employees of Samsung. Seo is prior art to the ’734 patent at least under 35 U.S.C. §§ 102(a), 102(b), and 102(e). Seo was not before the examiner during the prosecution.

Seo describes a “multimode data buffer.” Seo at Field of the Invention, 1:15–17. Just like the ’734 patent, Seo discloses a buffer with the ability to use either single-ended or differential data strobe signals. Jacob Decl. at ¶¶ 72–74. The type of signal used is chosen based on a “mode” of operation. Id. Seo specifically focuses on two of these modes: “single mode (SM)” and “dual mode (DM).” Id.

Seo’s description of these modes confirms that they represent single-ended and differential modes of signaling—the same two types of signaling the ’734 patent uses in the design of its data-strobe buffer. Id. As Seo states, “a single mode (SM)-type input buffer . . . compares a data strobe signal with a reference voltage,” whereas “a dual mode (DM)-type data strobe signal input buffer . . . compares a data strobe signal with the inverse signal of the data strobe signal instead of reference voltage.” Seo at 1:45–57; see also Jacob Decl. at ¶¶ 74–76.

Seo identifies the same problem as the ’734 patent, namely using a single memory controller connected to different types of DRAM memories that use different types of data strobe signals. See id. at 1:62–64 (“to satisfy demands of a variety of users, an SM/DM dual-use data strobe signal input buffer has been developed.”). Seo also provides the same solution as the ’734 patent—a data strobe
buffer with multiple “modes.” Jacob Decl. at ¶ 73. Seo discloses a data strobe buffer that “may operate in multiple modes, such as a single mode (SM) and a dual mode (DM),” where “the mode is selected by providing a signal.” Seo at Abstract. Seo’s concept of “modes” allows the memory controller to control different types of memory—in particular DDR DRAM that uses single-ended data strobe signals and DDR2 DRAM that use differential data strobe signals. Jacob Decl. at ¶ 74.

Even Seo’s description of the embodiments bears a close similarity to the claim language of the ’734 patent. Seo states:

Exemplary embodiments of the present invention are also directed to a data buffer including a differential amplifier circuit including at least two switches for passing an inverse data signal or a reference voltage, respectively, depending on a level of a control signal, and a differential amplifier for receiving a data signal, and either the inverse data signal or the reference voltage and outputting at least two different differentially amplified signals.

Id. at 2:37–44; Jacob Decl. at ¶ 75.

Seo makes clear that the data strobes contemplated are bi-directional, meaning that the memory controller produces the strobe signal on write operations, and the DRAM produces the strobe signal on read operations. Id. at ¶ 76. Seo discloses that the DRAM “uses a data strobe signal when the DRAM receives data from a memory controller or sends data to the memory controller.” ’734 patent at
1:37–39. For example, “in a data receiving operation, the DDR synchronous DRAM receives data with a data strobe signal from the memory controller.” *Id.* at 1:41–43. And, “in a data outputting operation, the DDR synchronous DRAM outputs data with a data strobe signal to the memory controller.” *Id.* at 1:43–45.

Seo discloses the following embodiment of the data strobe buffer capable of handling either a single-ended or differential data strobe, depending on mode:

![Diagram of Data Strobe Input Buffer](image)

As shown above, Figure 2 is “a block diagram of a data strobe input buffer according to an exemplary embodiment of the present invention.” *Id.* at Fig. 2, 7:46–48. This circuit shows three signals on the left-hand side: DQS (highlighted in blue), which transmits a data strobe signal; DQSB (highlighted in red), which transmits a data-strobe-bar signal or “inverse data signal”; and VREF (highlighted in red), which transmits a reference voltage. Jacob Decl. at ¶¶ 77–78.

This arrangement disclosed by Seo operates in two modes and supports both single-ended and differential data strobes, just like the ’734 patent. The differential amplifier 213 (highlighted in yellow) corresponds to the comparator in the ’734
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patent. The two switches for the CNTB/CNT, control and control-bar signals, (highlighted in blue) correspond to the selector in the ’734 patent. The switches receive the reference voltage and inverse data strobe, selects one, and outputs the selection to the selector, differential amplifier 213. *See id.* ¶¶ 78–82; ’734 patent at 7:61–8.8. This figure compares Seo Figure 2 with ’734 patent Figure 8A:

As in the ’734 patent, the selector “selects” either the reference voltage or inverse data strobe depending on the type of memory connected. Using this mechanism, it can use different operating modes for different types of memory.
For example, when the buffer receives a single-ended data-strobe signal, the selector “selects” and passes the reference voltage to the comparator. This operating mode could be used for DDR1 SDRAM. See Jacob Decl. ¶¶ 78–82.

On the other hand, when the buffer receives data and a data strobe signal, the selector “selects” and passes the inverse data strobe to the comparator. This operating mode can be used for DDR2 and DDR3 SDRAM. Thus, Seo addresses the same problem as the ’734 patent and solves it in the same way. The selector in Seo “selects” between two modes and allows the memory controller to use either single-ended or differential data strobes, just like the ’734 patent. See id.

B. U.S. Patent 7,173,871 (“Kong”)

U.S. Patent 7,173,871 (“Kong,” attached as Ex. 1104) was filed on March 19, 2003, issued on February 6, 2007. Kong was assigned to Samsung Electronics Co., Ltd. of Korea and lists Eun-Young Kong, Jun-Young Jeon, and Jae-Hyeong Lee as the inventors, who were all employees of Samsung. Kong is prior art to the ’734 patent at least under 35 U.S.C. §§ 102(a), 102(b), and 102(e). Kong was not before the examiner during the prosecution of the ’734 patent. Id.

Kong relates to a memory device containing a circuit for outputting a data strobe signal. Kong at Abstract, Field of the Invention, 1:14–18. Specifically, Kong discloses a “semiconductor memory device comprising at least two integrated circuits in which data is input and output in association with a reference (called a
data strobe signal) and a method for outputting the data strobe signal out of the semiconductor memory device.” *Id.* at 1:14–18, 2:61–65; Jacob Decl. at ¶ 84.

In Figure 3, Kong discloses the circuit for inputting/outputting the data strobe signal as illustrated below:

![Circuit Diagram](image)

Figure 3 shows “circuit diagrams of a data strobe signal input and output buffer and a control circuit contained in the semiconductor memory device.” Kong at 3:57–60. The specification describes Figure 3 in detail. *See id.* at Detailed Description of Preferred Embodiments, 4:8–5:51; Jacob Decl. at ¶¶ 85–87.

Unlike Seo, Kong discloses in detail the inner workings of a bi-directional data strobe signal *driver* capable of driving a data strobe signal through an input/output node for use as a timing signal. *Id.* at ¶¶ 86–87; *see also*, e.g., Kong at 1:13–19 (The invention relates to “a method for outputting the data strobe signal
out of the semiconductor memory device.”), 3:31–35 (“[T]he described embodiments provide methods of outputting, out of the semiconductor memory device, a data input/output reference signal, e.g., the data strobe signal generated from a DDR RAM.”); see also 1:13–18.

Like Seo, Kong discloses a receiver that receives incoming data strobe signals. In Seo, this is illustrated by the DQS node (highlighted in blue) which transmits the data strobe signal to differential amplifier 213, which then outputs the received data strobe signal as the DO signal, Jacob Decl. ¶ at 88:

Kong also discloses a data strobe receiver in Fig. 3 below. This is illustrated by the DQS node (highlighted in blue) which transmits the data strobe signal to inverter 32, which outputs the received data strobe signal as the DSI signal (highlighted in red). The only difference is that Kong—as a patent directed to the design of a circuit for outputting a data strobe signal—explicitly discloses the driver and its internal circuitry used to generate the data strobe signal. Jacob Decl. at ¶¶ 86–87
C. Seo and Kong Describe Same Data Strobe Buffer as ’734 Patent

The ’734 patent describes data strobe buffers from the perspective of the memory controller, whereas Seo and Kong describe data strobe buffers from the perspective of the memory device (such as DRAM). See Jacob Decl. at ¶¶ 89–92. This means, for example in Fig. 1 below, the ’734 patent describes a data strobe buffer contained within the memory controller on the left, whereas Seo and Kong describe data strobe buffers contained within the memory device on the right:
But this does not alter the invalidity analysis because the data strobe buffers (and relevant technologies and features) are the same. See id. It is akin to cars that drive on the left or right side of the road. Although the cars are oriented differently, they have the same components and work the same way.

The ’734 patent itself indicates that data strobe buffer components within the memory controller or memory device are the same. Figure 1 shows that the memory controller and memory device are symmetrical. Both have the same input/output nodes (P1/P3 for the memory controller and P2/P4 for the memory device). And both use the same DQS and DQ data strobe signals. Indeed, the data strobe signals are bi-directional (illustrated by left and right arrows), which means signals are both input and output between the memory controller and memory device. Thus, regardless of where the data strobe buffer is located (in the memory controller or memory device), it is used for both write and read operations.

The Patent Owner, Samsung, further supports that data strobe buffers components are the same. Although Seo is from the perspective of the memory device (such as DRAM), Samsung interprets it broadly include a data strobe buffer contained in the memory. In a pending district litigation, Samsung Electronics Co., Ltd. v. NVIDIA Corp., 3:14-cv-00757-REP (E.D. Va.), asserts Seo and alleges that certain products infringe claim 1 of Seo because they “include memory controllers.” See Ex. 1109 (Samsung’s Second Amended Complaint) at ¶¶ 2136–
53. Thus, Samsung’s own position is that the data strobe input buffer claimed in
Seo would read on a data strobe buffer contained in a memory controller as
described in the ’734 patent. The location and perspective of the data strobe buffer
does not alter the invalidity analysis. Jacob Decl. at ¶¶ 89–92.

The only difference between the ’734 patent and Seo and Kong is that the
terminology of read and write operations is reversed. When the ’734 patent
describes a write operation, it is from the perspective of the memory controller, so
it is equivalent to a read operation from the perspective of the memory device, as
described by Seo and Kong. Likewise, when the ’734 patent describes a read
operation, it is equivalent to a write operation in Seo and Kong. This is described
in further detail in ¶¶ 89–92 of Dr. Jacob’s declaration supporting this Petition.

VIII. MOTIVATION TO COMBINE THE PRIOR ART REFERENCES

A person of ordinary skill would have been strongly motivated to combine
the teachings of Seo and Kong, and vice versa, for many reasons. Id. at ¶¶ 99–106.

1. Same Corporation and Same Memory Technology

First, Seo, Kong and the ’734 patent are all patents from the same
company—Samsung—and describe the same Samsung memory technology and
features. Id. at ¶ 95. In Ex parte Mettke, the BPAI ruled that there was “motivation
to combine any of the teachings” of four prior art references to invalidate a claim
because they are “from the same corporation, and expressly teach modifications,
variations, and improvements to a pay-for-use public communications terminal.”

Ex. 1108 (Ex Parte Mettke, No. 2008-0610, 2008 WL 4448201, at *17 (BPAI Sept. 30, 2008), aff’d, 570 F.3d 1356 (Fed. Cir. 2009)). And because the four prior art references “are all from the same corporation and all relate to versions of the same pay-for-use terminal,” a person of ordinary skill “would have been motivated to combine the teachings in one reference with teaching in another reference . . . .” Id. Further, because the references are from the same corporation, “there is not the usual obviousness problem of explaining why one skilled in the art would have sought to combine two references from unrelated sources.” Id.

Here, both Seo and Kong are from Samsung and discuss the same Samsung memory technology and features as claimed and disclosed in the ’734 patent. See Jacob Decl. at ¶ 95. The inventors of both Seo and Kong were all employees of Samsung in Korea. Seo and Kong were also filed around the same time in 2002. Id. It is likely that the Samsung engineers involved would have known of each other’s work. Id. Certainly, the listed inventors to the Seo and Kong patents qualify as persons of ordinary skill in the art and would have presumptively known of each other’s work. Working at the same company and on the same technology would have further motivated them to incorporate each other’s work with their own to obtain design efficiency and reduce time to market. Id. ¶¶ 95–96.

Indeed, it is likely that the memory technologies and features described in
Seo and Kong were in fact already combined at Samsung. This is further supported because Kong cites to Seo on the face of the patent. See Optivus Technology, v. Ion Beam Applications, 469 F.3d 978, 990–91 (Fed. Cir. 2006) (finding motivation to combine where prior art reference mentioned another prior art reference).

2. Same Field

Second, Seo and Kong both relate to the same field of computer memory, and specifically to read and write operations from the perspective of DDR DRAM memory. Id. at ¶ 97. Seo relates to a “memory device and, more particularly, to a multimode data buffer” which “operates as a DDR synchronous DRAM.” Seo at 1:15-17, 15:23–25. Kong discloses “memory device and a method for outputting the data strobe signal out of the semiconductor memory device,” which can include “the data strobe signal generated from a DDR RAM.” Kong at 1:13–18, 3:34–35.

In DDR DRAM systems, memory devices use bi-directional data strobe buffers. Id. at ¶¶ 97–98. Due to the common features of these circuits, a person of ordinary skill would readily look to the complementary features of other references for more information and recognize that these disclosures are readily combined, and would have been motivated to combine them to develop a circuit compatible with DDR DRAM memory standards. See id. at ¶¶ 98–101.

3. Same Problem/Same Solution

Third, both Seo and Kong address the same technical problem and solution
of developing input/output buffers for bi-directional data strobes. *Id.* at ¶¶ 101–102. For example, Figure 3 of Kong explicitly discloses the internal configuration of a data-strobe input/output buffer. *Id.*; Kong at 3:57-60.

The “driver component” (highlighted in green) outputs or drives data strobe signal DQS (highlighted in blue) to the “receiver component” (highlighted in orange) that receives the data strobe signal DQS. *Id.* at ¶¶ 102–105. The figure shows both the driver and receiver components connected to the DQS data strobe signal. *Id.*

Seo discloses a receiver identical to the receiver Kong, except the Seo receiver is capable of handling single-ended and differential signaling. Seo at 7:48–50; Jacob Decl. at ¶¶ 105–06. A person of ordinary skill would have readily recognized that the receiver in Kong could be replaced by the receiver in Seo. *Id.* By combining the driver functionality of Kong with the Seo receiver, the device would then be capable of handling both single-ended and differential signaling. *Id.*
The figure above shows how the receiver in Kong would be removed, and where the complementary Seo receiver would naturally be added. The figure below shows the combined invention of the Seo receiver connected to the Kong driver (with the Seo receiver rotated 180 degrees but same internal configuration):
Likewise, when provided with the receiver disclosed in Seo, a person of ordinary skill in the art would be motivated to combine it with the driver disclosed in Kong. Jacob Decl. at ¶ 106. While Seo teaches the process of receiving the data strobe, it does not specifically describe the internal configuration of the driver responsible for driving or generating the data strobe signal—which is exactly what Kong teaches. In the figure below, one of Kong’s data strobe driver circuits could be added to each of Seo’s DQS and DQSB nodes to combine Kong’s driver with Seo’s receiver, e.g., Kong at 1:13-18; see also Jacob Decl. at ¶¶ 104–06:

Thus, because Kong provides the complementary driver component already referenced in Seo, and the two references address exactly the same technology—developing I/O buffers for bi-directional data strobes—a person of ordinary skill would have been readily motivated to combine both Seo and Kong. Id.
4. Nothing Incompatible

Finally, nothing in either Seo or Kong teaches away from their combination. Both disclose data strobe buffers contained in the memory device (DRAM) and are described from that perspective. To the extent there are any implementation differences between the two references, they were merely design choices, and the driver disclosed in Kong would fit into the receiver disclosed in Seo, and the receiver disclosed in Seo would fit into the driver disclosed in Kong. See id. at ¶¶ 102–06. There is no essential feature in Seo in conflict with an essential feature of Kong, and that the two references are a natural fit. Id. This is further supported because Kong and Seo are from the same company (Samsung), were developed at the same place and time, and because Kong cites to Seo on the face of the patent.

IX. ’734 PROSECUTION HISTORY

The ’734 prosecution history is attached as Ex. 1102. The Examiner considered a single U.S. patent application (U.S. Patent Appl. 2004/0196725) and three Japanese patents (JP 2002007200, JP 2005353168, and JP 2006059046) during the prosecution of the ’734 patent. The Examiner did not consider Seo or Kong, the prior art that are the subject of this IPR. The prior art references that were cited during prosecution are limited, and do not contain the same disclosures of Seo and Kong discussed in this IPR. Thus, the Examiner did not rely on the cited prior art to reject the claims of the ’734 patent during prosecution.
X. PRECISE REASONS FOR THE RELIEF REQUESTED

Claims 1, 7–9, 12, 13, 17, and 19 of the ’734 patent are subject to this *inter partes* review. Jacob Decl. at ¶ 121. These claims are invalid under 35 U.S.C. § 103 because they are rendered obvious by Seo in view of Kong. *Id.*

XI. GROUNDS OF INVALIDITY

A. Claim 1

a. “a data strobe buffer comprising: a first input/output node; a first driver coupled to the first input/output node,”

Seo discloses a data strobe buffer. Seo at Abstract (“A data buffer, such as a data strobe input buffer, which may operate in multiple modes . . . ”). Seo also discloses a data strobe buffer comprising a first input/output node. Input/output node means “a point in a circuit through which signals may be input and/or output.” *Id.* at ¶¶ 118–20. Seo discloses a DQS node as an input/output node (highlighted in blue below) because it is the point through which the DQS signal is transmitted. *Id.* at ¶¶ 122–125:

See Seo at Fig. 2, 7:46–8:8 (“Fig. 2 is a block diagram of a data strobe input buffer according to an exemplary embodiment of the present invention”), 7:53–54 (“data
strobe input buffer 13 differentially amplifies a data strobe signal (DQS)).

Kong also discloses a first driver coupled to the first input/output node:

Jacob Decl. at ¶ 123. Figure 3 of Kong shows the internal configuration of a data-strobe input/output buffer, in which a tri-state buffer (34) is connected to the DQS input/output node, and the controller for that tri-state buffer (20-1) is connected to the tri-state buffer, together making a data-strobe driver, the driver components highlighted in green. Id. at ¶ 124. The first input/output node corresponds to the DQS pin, highlighted in blue, which sends and receives the data strobe signal DQS. See Kong at 4:54–67; Jacob Decl. at ¶ 124.

In both references, the first input/output node corresponds to the DQS pin, highlighted in blue, over which data strobe signal DQS is transmitted. Id. at ¶ 125.

b. “the first driver configured to output a first data strobe signal to the first input/output node during a write operation;”
Kong discloses that the first driver is configured to output a first data strobe signal (the DQS signal) to the first input/output node (DQS pin) during a write operation. *Id.* at ¶¶ 126–128. Figures 1 and 2 from Kong disclose a system where: (1) during write operations, the data strobe input/output buffers receive an incoming data strobe signal from an external input/output pin; and (2) during read operations, the data strobe input/output buffers generate the outgoing data strobe signal through the external input/output pin. *See* Kong at 1:55–62. The figures below, Kong, shows Kong in Fig. 2 contains identical components as Fig. 1:

![Fig. 1](image1)

![Fig. 2](image2)

Specifically, Kong discloses that Figure 1 from Kong is “block diagram of a conventional semiconductor memory device 100 comprising first and second integrated circuits 110-1 and 110-2.” *Id.* at 1:39–41. Kong further discloses that the integrated circuits include “data strobe signal pads 12-1 and 12-2,” and “data
strobe signal input and output buffers (DQSBs) 116-1 and 116-2.” 

Kong states that “the semiconductor memory device includes a data strobe signal (DQS) pin 11,” and that this pin “is commonly connected to the data strobe signal pads 12-1 and 12-2 formed in the first and second integrated circuits 110-1 and 110-2.” 

Kong describes the behavior of write operations, in which “the data strobe signal input/output buffers 116-1 and 116-2 each receive and buffer the data strobe signal DQS,” and that, on writes, the external data strobe signal DQS is “input through the external data strobe signal input and output pin 11 to generate input data strobe signal DSI.” 

Kong also describes the behavior of read operations, where “internally generated” “output data strobe signal DSO” is used to generate the external outgoing data strobe signal, “the data strobe signal DQS.”

As described in section VII.C above, when Kong discloses a “read” operation in which the data strobe is output, this corresponds to a “write” operation in the ’734 patent, in which the data strobe is output.

Thus, data strobe signal DQS is output during a write operation.

c. “and a first receiver coupled to receive a second data strobe signal from the first input/output node and output a third data strobe signal”

Seo discloses a first receiver coupled (element 21) coupled to receive a
second data strobe signal (DQS signal) from the first input/output node (DQS pin) and output a third data strobe signal (DO).

See Seo at 7:46–8:8; Jacob Decl. at ¶ 129.

The first receiver is highlighted in orange and corresponds to the differential amplification circuit 21. Id. at ¶ 130. The first input/output node is highlighted in blue and corresponds to the DQS pin. Id. The second data strobe signal corresponds to the received data strobe signal. The third data strobe signal is highlighted in red and corresponds to DO. Id.; Seo at 7:46–8:8.

The figure and specification shows the incoming data strobe signal (the “second” strobe signal) received from the DQS input/output node (in blue) that sends the DQS signal to the data strobe input buffer 13, which contains the differential amplification circuit 21, highlighted in orange. Jacob Decl. at ¶ 131. The “third” strobe signal, which is output by the differential amplification circuit, is labeled “DO” in the figure. Id.

d. “during a read operation when the data strobe buffer is in a first or second mode,”
Kong discloses this limitation as discussed and analyzed for claim limitation 1(b) on pages 37–38 above. Jacob Decl. at ¶¶ 132–34; Kong at Fig. 1–2, 1:39–2:3.

As described above, when Kong discloses a “write” operation in which the data strobe is received, this corresponds to a “read” operation in the ’734 patent, in which the data strobe is received. Jacob Decl. at ¶ 133. Thus, the DQS data-strobe signal is received during a read operation. Id. at ¶ 134.

e. “the first receiver configured to compare the second data strobe signal with a first reference voltage and output a result of the comparison as the third data strobe signal when the data strobe buffer is in the first mode, the receiver further configured to not compare the second data strobe signal with the first reference voltage when the data strobe buffer is in the second mode.”

Seo discloses the first receiver (element 21) configured to compare the second data strobe signal (DQSB) with a first reference voltage (VREF) and output a result of the comparison as the third data strobe signal (DO) when the buffer is in a first mode. The receiver is configured to not perform the comparison when the data strobe buffer is in the second mode. This is illustrated by Figure 2 below:
See Seo at 7:46–8:8; Jacob Decl. at ¶ 135. The first receiver corresponds to the differential amplification circuit 21, which is highlighted in orange. Id. at ¶ 136. The second data strobe signal corresponds to the received DQS signal, which is highlighted in blue. Id. The first reference voltage corresponds to VREF, which is highlighted in purple. Id. The third data strobe signal corresponds to DO, which is highlighted in red. Id.; see also Seo at 7:46–8:8.

As the figure and specification shows, switches 211 and 212 select between the inputs VREF and DQSB. Id. at 7:53; Jacob Decl. at ¶ 137. The switches pass the selected input on to their output, where it is fed into differential amplifier 213 along with the data strobe DQS. Id. Whether switches 211 and 212 select VREF or DQSB depends on the state of the CNT/CNTB signals (CNTB is simply the inverse of CNT). Id. Thus, the data-strobe receiver 21 generates its output, the “third” data strobe signal DO, either by comparing DQS against DQSB or by comparing DQS against VREF. Id. The comparison is performed in differential amplifier 213, and the CNT/CNTB signals determine whether the comparison is between DQS and DQSB or between DQS and VREF. See Seo at 7:46–8:8.

Seo discloses that, in single mode (SM), the differential amplifier 213 compares the data strobe signal DQS to the reference voltage VREF, and in dual mode (DM), the differential amplifier 213 compares the data strobe signal DQS to the inverse data strobe signal DQSB. Jacob Decl. at ¶ 138. When the CNT control
signal is in a first state (e.g. logic 1 or “high”) “the switch 211 is turned on and the switch 212 is turned off.” Seo at 7:61–63; Jacob Decl. at ¶ 138. In this state, “the differential amplifier 213 differentially amplifies the data strobe signal (DQS) and the reference voltage (VREF)” to produce the DO output signal. *Id.* at 7:63–65. This describes operation in “the single mode (SM).” *Id.* at 7:66–67.

When the CNT control signal is in a second state (e.g., logic 0 or “low”), “the switch 212 is turned on, and the switch 211 is turned off.” Seo at 8:1–4; Jacob Decl. at ¶ 139. In this state, “the differential amplifier 213 differentially amplifies the data strobe signal (DQS) and the inverse data strobe signal (DQSB)” to produce the DO output signal. Seo at 8:4–7. This describes operation in “dual mode (DM).” *Id.* at 8:7–8.

As Seo discloses, if the data strobe input buffer is in a first mode, the output of the differential amplifier 213 is the comparison between the data strobe signal (DQS) and the reference voltage (VREF). Jacob Decl. at ¶ 140. But if the data strobe input buffer is in a second mode, the output of the differential amplifier 213 is the comparison between the data strobe signal (DQS) and its complement data strobe signal (DQSB)—i.e., in this second mode, the receiver does *not* compare the second data strobe signal with the reference voltage. *Id.*; see Seo at 8:1–8.

In addition to the reasons discussed above in the motivation to combine section in section VIII above, a person of ordinary skill would have been motivated
to look to Kong for guidance about input/out nodes and a first driver because Seo and Kong are from the same company, are contemporary of each other, Kong cites to Seo on the face of the patent, and the two patents address the same technical problem and solution of developing input/output buffers for bi-directional data strobes. *See also* Jacob Decl. at ¶ 141. Moreover, Kong discloses precisely those circuits and their implementation details, such as one of the most common ways to implement a tri-state buffer. *Id.; see also* Kong at 4:57–64.

Thus, Seo in view of Kong discloses all of the elements of Claim 1 and thus renders the claim obvious. Jacob Decl. at ¶ 142.

**B. Claim 7:** “The data strobe buffer of claim 1, wherein the first receiver includes a comparator, a first input of the comparator coupled to the first input/output node, the third data strobe signal being output from the comparator.”

As discussed above for Claim 1, Seo discloses a data strobe buffer. *See also* Jacob Decl. at ¶ 143. As further discussed above, Seo discloses that the first receiver is the differential amplification circuit 21, as shown in Figure 2:

*See Seo at Fig. 2, 7:46–8:8. The first receiver corresponds to the differential...
amplification circuit 21, highlighted in green. Jacob Decl. at ¶ 144. The comparator corresponds to the differential amplifier 213, highlighted in orange. Id. The first input of comparator is highlighted in purple. Id. The first input/output node corresponds to DQS pin, and is highlighted in blue. Id. The second data strobe corresponds to the received DQS signal. Id. The third data strobe corresponds to DO, highlighted in red. Id.; see also Seo at 7:46–8:8.

The figure and specification shows the incoming data strobe signal (the “second” strobe signal) received from the DQS input/output node (highlighted in blue) that sends the DQS signal to the data strobe input buffer 13, which contains the differential amplification circuit 21 (highlighted in purple). Jacob Decl. at ¶ 145. As the figure shows, the differential amplification circuit 21 (the claimed first receiver), includes a comparator (differential amplifier 213) with an input coupled to the first input/output node DQS. Id. The third data strobe signal, labeled “DO,” is output by the differential amplification circuit (the claimed comparator). Id.

Seo thus discloses all of the elements of Claim 7. Since Claim 7 is dependent on Claim 1, Seo in view of Kong renders Claim 7 obvious. Id. at ¶ 146.

C. **Claim 8:** “The data strobe buffer of claim 7, wherein the first receiver further includes a first selector, an output of the first selector coupled to a second input of the comparator.”

As discussed above for Claim 7, Seo discloses a data strobe buffer. As further disclosed, Seo also discloses that the first receiver is the differential
amplification circuit 21, as shown in Figure 2 of Seo:

See Seo at 7:46–8:8; Jacob Decl. at ¶ 147. The first receiver, highlighted in orange, corresponds to the differential amplification circuit 21. *Id.* at ¶ 148. The comparator corresponds to differential amplifier 213, highlighted in yellow. *Id.* The first input of the comparator is highlighted in purple and the second input is highlighted in turquoise. *Id.* The first selector corresponds to switches 211 and 212, highlighted in grey. *Id.*; *see also* Seo at 7:46–8:8.

As the figure and specification shows, the differential amplification circuit 21 (the claimed first receiver) includes a selector (switches 211 and 212, highlighted in grey), whose output is coupled to the *second* input to differential amplifier 213, highlighted in purple, the second input highlighted in yellow. Jacob Decl. at ¶ 149. The first input to the differential amplifier 213 is the DQS signal, highlighted in purple. *Id.*; *see also* Seo at 7:46–8:8.

Seo thus discloses all of the elements of Claim 8. Since Claim 8 is dependent on Claim 1, Seo in view of Kong renders claim 8 obvious. *Id.* at ¶ 150.
D. Claim 9: “The data strobe buffer of claim 8, wherein the first selector is an analog multiplexer.”

As described above for Claim 8, Seo discloses a data strobe buffer. See also id. at ¶ 151. As further described above, Seo discloses that the claimed first selector, which corresponds to switches 211 and 212 in the differential amplification circuit 21 (the claimed first receiver), is illustrated in Figure 2:

See Seo at 7:46–8:8. The first receiver corresponds to the differential amplification circuit 21, highlighted in orange. Jacob Decl. at ¶ 152. The comparator corresponds to differential amplifier 213, highlighted in yellow. Id. The first and second inputs of the comparator are highlighted in purple and turquoise, respectively. Id. The first selector corresponds to switches 211 and 212, highlighted in grey. Id.

The pair of switches 211 and 212 is shown in detail in Figure 3A:
See id. at 8:9–21. Seo states that Figure 3A is a block diagram of “switches 211 and 212 according to an exemplary embodiment of the present invention, where each switch 211, 212 is implemented as a transmission gate.” Id. at 8:9–11. As the figure shows, this is an analog multiplexer in which “each transmission gate receives the control signal (CNT) and the inverse control signal (CNTB),” and the multiplexer passes “either the inverse data strobe signal (DQSB) or the reference voltage (VREF)” to its output, depending on the state of the CNT/CNTB signals. Id. at 8:12–15. The timing of the output is “triggered by the leading edge of a pulse of the control signal (CNT) and the inverse control signal (CNTB).” Id. at 8:17–18.

Seo discloses all of the elements of Claim 9. Since Claim 9 is dependent on Claim 1, Seo in view of Kong renders Claim 9 obvious. Jacob Decl. at ¶ 154–55.

E. Claim 12

a. “The data strobe buffer of claim 8, further comprising: a second input/output node”;

Seo discloses a data strobe buffer of claim 8 comprising a second input/output node (the DQSB pin) in Figure 2 below:
Seo at 7:46–8:8; Jacob Decl. at ¶ 157. The first input/output node, highlighted in blue, corresponds to the DQS pin. *Id.* The second input/output node, highlighted in brown, is the DQSB pin. *Id.*

b. “and a second driver coupled to the second input/output node,”

Each of the DQS and DQSB pins, when handling a bi-directional data strobe, would have an input/output buffer coupled to it, which is the driver portion described in Kong. *Id.* at ¶ 158. Kong discloses this limitation in Figure 3. *Id.* The second input/output node, highlighted in blue, is DQS. *Id.* at ¶ 159. The second driver, highlighted in green, is the output buffer in 20-1 and 34. Kong at 4:54–67:

c. “the second driver configured to output a first data strobe bar signal to the second input/output node during the write operation, the first data strobe bar signal being an inversion of the first data strobe signal,”
Kong discloses this limitation as discussed and analyzed for claim limitation 1(b) on pages 37–38 above. Jacob Decl. at ¶¶ 160–63; Kong at Fig. 1–2, 1:39–2:3.

d. “and the second input/output node coupled to an input of the first selector.”

As discussed above, the second input/output node is DQSB, and the first selector are switches 211 and 212. Jacob Decl. at ¶ 164. As shown in Seo Fig. 2, the second input/output node DQSB is coupled to switch 212 of the first selector:

See Seo at 7:46–8:8. The differential amplification circuit 21, highlighted in orange, is the first receiver. Jacob Decl. at ¶ 165. The differential amplifier 213, highlighted in yellow, is the comparator. Id. The first selector corresponds to switches 211 and 212, highlighted in grey. Id. The second input/output node is the DQSB pin, highlighted in brown. Id.; see also Seo at 7:46–8:8.

Thus, the second input/output node, DQSB, is coupled to an input of the first selector. Jacob Decl. at ¶ 166. As discussed in detail in claim 1 above, a person of ordinary skill in the art would have been motivated to look to Kong for guidance about input/output nodes, a first driver, and a second driver. Id. at ¶ 167.
Thus, Seo in view of Kong discloses all of the elements of Claim 12 and renders it obvious. *Id.* at 168.

**F. Claim 13**

e. “The data strobe buffer of claim 12, the first input/output node configured to receive the second data strobe signal during the read operation, the second input/output node configured to receive a second data strobe bar signal during the read operation,”

As described in Claims 1 and 12, and as shown in Seo Figure 2, the claimed first input/output node is DQS (highlighted in blue); the second data strobe signal is the received DQS signal; the second input/output node is DQSB (highlighted in brown); and the second data strobe bar signal is the received DQSB signal:

![Diagram](image)

Seo at Fig. 2, 7:46–8:8; *see also* Jacob Decl. at ¶ 169. The first input/output node corresponds to the DQS pin, (in blue above). *Id.* at ¶ 170. The second input/output node corresponds to the DQSB pin, highlighted in brown. *Id.*; Seo at 7:46–8:8. Kong also discloses Claim 13 as discussed and analyzed for claim limitation 1(b) on pages 37–38 above. Jacob Decl. at ¶¶ 160–63; Kong at Fig. 1–2, 1:39–2:3.

f. “and the first selector being configured to output the second data strobe bar signal to the second input of the comparator”
As described above for Claim 8, the claimed first selector, which corresponds to switches 211 and 212 in the differential amplification circuit 21 (the claimed first receiver), is illustrated in Figure 2 of Seo:

See Seo at Fig. 2, 7:46–8:8; Jacob Decl. at ¶ 175. The first receiver is differential amplification circuit 21, highlighted in orange. *Id.* at ¶ 176. The comparator corresponds to differential amplifier 213, highlighted in yellow. *Id.* The first and second inputs of the comparator are highlighted in purple and turquoise. *Id.* The first selector corresponds to switches 211 and 212, highlighted in gray. *Id.*

Seo describes how, in the dual mode (DM), the second data strobe bar signal (DQSB) is transmitted through switch 212 of the first selector to the second input (highlighted in yellow) of the comparator (differential amplifier 213) to produce the output, labeled DO. *Id.* at ¶ 177. When the CNT signal is in a logic 0 or “low” state, “switch 212 is turned on, and the switch 211 is turned off.” *Id.* at 8:1–8. In this state, the DQSB signal is passed to the differential amplifier 213, and as a result “the differential amplifier 213 differentially amplifies the data strobe signal (DQS) and the inverse data strobe signal (DQSB),” to produce “the differentially
amplified signal (DO)” output signal. *Id.* This is “operation in the dual mode (DM).” *Id.; see also* Jacob Decl. at ¶ 177.

Thus, in dual mode (DM), the claimed selector (switches 211 and 212) outputs the DQSB signal (the claimed second data strobe bar signal) to differential amplifier 213, which corresponds to the claimed comparator. *Id.* at ¶ 178.

g. “*during the read operation when the data strobe buffer is in the second mode.*”

As described above, for claim element 13(a) above, the signal is received during a read operation. *See also* Jacob Decl. at ¶ 179. As also described for claim element 13(b) above, the claimed second mode is Seo’s dual mode (DM). *Id.*

As discussed in detail in claim 1 above, a person of ordinary skill in the art would have been motivated to look to Kong for guidance about input/output nodes, a first driver, and a second driver. *See also* id. at ¶ 180.

Thus, Seo in combination with Kong discloses all of the elements of Claim 13 and renders the claim obvious. *Id.* at ¶ 181.

G. Claim 17

a. “A data strobe buffer comprising: a first input/output node; a second input/output node;

Seo discusses a data strobe buffer as discussed in claim 1 above, and it comprises a first/input/output node (DQS pin) and a second input/output node (DQSB pin). These are illustrated in Figure 2 below:
See Seo at Fig. 2, 7:46–8:8; Jacob Decl. at ¶ 182. The first input/output node corresponds to DQSB pin, highlighted in brown, which sends and receives the complementary data-strobe signal DQSB. *Id.* at ¶ 183. The second input/output node corresponds to DQS pin, highlighted in blue, which sends and receives the data strobe signal DQS. *Id.; see also* Seo at 7:46–8:8.

b. **“a driver coupled to the first input/output node,”**

Each of the DQS and DQSB pins, when handling a bi-directional data strobe, would have an input/output buffer coupled to it, the driver portion described in Kong. Jacob Decl. at ¶ 184. Kong discloses this limitation in Figure 3:
Figure 3 shows the internals of a data strobe input/output buffer in which a data-strobe driver (the driver components, highlighted in green) includes a tri-state buffer 34, which is connected to the DQS input/output node (which corresponds to the DQSB pin in the previous diagram). Id. at ¶ 185; Kong at 4:54–67.

c. “configured to output a first data strobe signal to the first input/output node during a write operation;”.

Kong discloses this limitation as discussed and analyzed for claim limitation 1(b) on pages 37–38 above. Jacob Decl. at ¶¶ 160–63; Kong at Fig. 1–2, 1:39–2:3.

d. “and a receiver coupled to receive a second data strobe signal from the second input/output node and output a third data strobe signal during a read operation when the data strobe buffer is in a first or second mode,”

Seo discloses this limitation in Figure 2 and the specification:

See Seo at 7:46–8:8; Jacob Decl. at ¶ 190. The first input/output node corresponds to the DQSB pin, highlighted in brown, which is used to send and receive the complementary data strobe signal DQSB. Id. at ¶ 191. The second input/output node corresponds to the DQS pin, highlighted in blue, which is used to send and receive the data strobe signal DQS. Id. The receiver, highlighted in orange,
corresponds to the differential amplification circuit 21 and receives the second data strobe signal (the received DQS signal that arrives on the DQS pin) from the second input/output node, the DQS pin. Id. The third data strobe signal corresponds to the DO signal, highlighted in red. Id.; see also Seo at 7:46–8:8.

As described in detail above, this limitation is disclosed for the same reasons as set forth as to limitation [1b] of claim 1. Jacob Decl. at ¶¶ 192–95.

e. “the first receiver configured to compare the second data strobe signal with a first reference voltage and output a result of the comparison as the third data strobe signal when the data strobe buffer is in the first mode,”

Seo discloses the first receiver (element 21) configured to compare the second data strobe signal (DQSB signal) with a first reference voltage (VREF) and output a result of the comparison as the third data strobe signal (DO signal) when the data strobe buffer is in the first mode, as seen in Figure 2:

See Seo at 7:46–8:8; Jacob Decl. at ¶ 196. The first input/output node corresponds to the DQSB pin, highlighted in brown. Id. at ¶ 197. The second input/output node
corresponds to the DQS pin, highlighted in blue. *Id.* The receiver corresponds to the differential amplification circuit 21, highlighted in orange. *Id.* The second data strobe signal corresponds to the received DQS signal. *Id.* The third data strobe signal corresponds to the DO signal, highlighted in red. The first reference voltage, highlighted in purple, is VREF. *Id.*; see also Seo at 7:46–8:8.

As the figure and specification shows, switches 211 and 212 select between two inputs: VREF and DQSB. *Id.* at 7:53; Jacob Decl. at ¶ 198. The switches pass the selected input on to their output, where it is fed along with data strobe signal DQS into differential amplifier 213. Seo at 7:53. Whether switches 211 and 212 choose VREF or DQSB depends on the state of the CNT/CNTB signals (CNTB is simply the inverse of CNT). *Id.* Thus, data-strobe receiver 21 generates its output, the “third” data-strobe signal DO, either by comparing DQS against DQSB or by comparing DQS against VREF. *Id.* The comparison is performed in differential amplifier 213, and the CNT/CNTB signals determine whether it is between DQS and DQSB or between DQS and VREF. *Id.*; see also Jacob Decl. at ¶ 198.

Seo discloses that, in single mode (SM), the differential amplifier 213 compares the data strobe signal DQS to the reference voltage VREF, and in dual mode (DM), the differential amplifier 213 compares the data strobe signal DQS to the inverse data strobe signal DQSB. *Id.* at ¶ 199. When the CNT control signal is in a first state (e.g., logic 1 or “high”), “switch 211 is turned on and the switch 212
is turned off.” Seo at 7:61–63. In this state, “the differential amplifier 213
differentially amplifies the data strobe signal (DQS) and the reference voltage
(VREF)” to produce the DO output signal. Id. at 7:63–66. This describes
“operation in the single mode (SM).” Id. at 7:66–67. When the CNT signal is in a
second state (e.g., logic 0 or “low”), “switch 212 is turned on, and the switch 211 is
turned off.” Id. at 8:1–4. In this state, “the differential amplifier 213 differentially
amplifies the data strobe signal (DQS) and the inverse data strobe signal (DQSB),”
to produce output signal DO. Id. at 8:4–6. This is “operation in the dual mode
(DM).” Id. at 8:6–8; see also Jacob Decl. at ¶ 199.

As Seo discloses, if the data strobe input buffer is in a first mode, then the
output of the differential amplifier 213 is the comparison between the data strobe
signal (DQS) and the reference voltage (VREF); however, when it is in second
mode, the output of the differential amplifier 213 is the comparison between data
strobe signal (DQS) and its complement data strobe signal DQSB—i.e., in second
mode, the receiver does not compare the second data strobe signal with the
reference voltage. Id. at ¶ 200.

As discussed in detail in Claim 1 above, a person of ordinary skill would
have been motivated to look to Kong for guidance about input/output nodes, and
drivers. See Jacob Decl. at ¶ 201. Thus, Seo in view of Kong discloses all of the
elements of Claim 17 and thus renders the claim obvious. Id. at ¶ 202.
H. Claim 19: “The data strobe buffer of claim 17, the receiver further includes a selector and comparator, an output of the selector coupled to an input of the comparator.”

As described above for Claim 17, Seo discloses data strobe buffer containing a receiver, and seen in Figure 2:

See Seo at 7:46–8:8; Jacob Decl. at ¶ 203. The differential amplification circuit 21, highlighted in orange, corresponds to the receiver. *ld.* at ¶ 204. The selector corresponds to switches 211 and 212, highlighted in grey. *ld.* The output of the selector and input of the comparator are highlighted in turquoise. The comparator corresponds to the differential amplifier 213, highlighted in purple. Seo at 7:46–8:8; Jacob Decl. at ¶ 204. As the figure and specification shows, the differential amplification circuit 21 (the claimed first receiver) includes a selector (switches 211 and 212, highlighted in grey), whose output is coupled to an input of the comparator (differential amplifier 213, highlighted in orange). *ld.* at ¶ 205.

Seo discloses all of the elements of Claim 19. Since Claim 19 is dependent on Claim 17, Seo in view of Kong renders Claim 19 obvious. *ld.* at ¶ 206.
XII. CONCLUSION

For the reasons set forth above, *inter partes* review of claims 1, 7–9, 12, 13, 17, and 19 of the ’734 patent is requested.

Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned certifies that a complete copy of this Petition for *Inter Partes* Review of U.S. Patent No. 7,804,734 and all Exhibits and other documents filed together with this Petition were served on the official correspondence address for U.S. Patent No. 7,804,734 shown in PAIR and Samsung Electronics Co., Ltd.’s current patent counsel:

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