UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SONY CORPORATION, SAMSUNG ELECTRONICS CO., LTD.,
SAMSUNG DISPLAY CO., LTD

Petitioners

Patent No. 7,202,843
Issue Date: April 10, 2007
Title: DRIVING CIRCUIT OF A LIQUID CRYSTAL DISPLAY PANEL AND RELATED DRIVING METHOD

PETITION FOR INTER PARTES REVIEW

OF U.S. PATENT NO. 7,202,843

No. IPR2015-00862
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I. Mandatory Notices (37 C.F.R. § 42.8)


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II. Grounds for Standing (37 C.F.R. § 42.104(a))

Petitioners certify that the patent for which review is sought, U.S. Patent No. 7,202,843 (“the ’843 Patent,” Sony-1001), is available for inter partes review and that Petitioners are not barred or estopped from requesting an inter partes review challenging the patent claims on the grounds identified in this petition.
III. Identification of Challenge (37 C.F.R. § 42.104(b)(1)-(3)) and Relief Requested (37 C.F.R. § 42.22(a)(1))

Petitioners challenge claims 1-3 of the ‘843 Patent under 35 U.S.C. § 103. Cancellation of those claims is requested. In support of the following grounds, Petitioners submit the declaration of technical expert Thomas Credelle (Sony-1015).

A. Background of the ‘843 Patent

The ‘843 Patent describes the invention as a driving circuit of a liquid crystal display (LCD) panel, and more particularly a driving circuit and method for decreasing the reaction time of a liquid crystal element by applying two data impulses to a pixel electrode within one frame period. ’843 Patent at 1:8-12.

According to the ‘843 Patent, LCD devices have a disadvantage compared to traditional Cathode Ray Tube (CRT) displays due to the characteristics of liquid crystal molecules. Id. at 1:20-24. To drive a pixel in an LCD device, a driving circuit applies a charge which corresponds to the desired gray level for the pixel. Id. at 1:39-52. The charge causes the pixel’s liquid crystal molecules to “twist” to a desired transmission rate (i.e., brightness level). Id. at 1:19-24, 1:53-65. The driving circuit outputs the appropriate charge based on input frame data, which defines the gray level that each pixel must reach within a frame period. Id. at 1:27-35. However, “[t]here is a time delay when charging liquid crystal molecules. . . . Such a delay causes blurring.” Id. at 1:62-2:2. The ‘843 Patent describes that in order to address the blurring issue, “some conventional LCD are overdriven, which means applying a higher or a lower
data impulse to the pixel electrode to accelerate the reaction speed of the liquid crystal molecules, so that the pixel can reach the predetermined gray level in a predetermined frame period.” Id. at 2:2-7. While the overdrive technique improves the reaction speed of liquid crystal molecules, the ‘843 Patent alleges that the desired transmission rate still cannot be reached within one frame period, thus the blurring issue persists. Id. at 2:7-12. The ‘843 Patent purports to address the blurring issue by providing a driving circuit that generates and applies a plurality of overdriven data impulses (i.e., charges) to each pixel of an LCD device within a single frame period. Id. at 2:33-48. In the driving circuit, a source driver “generate[s] corresponding data line voltages . . . according to the plurality of overdriven data included in the frame signals G in order to drive the LCD panel.” Id. at 3:28-36. Thus, the data impulses are voltages applied to the pixels of the LCD panel. Credelle Decl. at ¶ 29. The overdriven data impulses are generated by comparing the input frame data for the current frame period with delayed frame data for the preceding frame period; the delayed frame data is stored in a memory device. Id. at 2:33-40, 4:49-55; 5:11-13.

B. Printed Publications Relied On

Petitioners rely on the following patents and publications:


Suzuki was filed on September 30, 2002 and published on August 21, 2003, and is prior art to the ’843 Patent under at least 35 U.S.C. § 102(e). Suzuki was not cited
during the prosecution of the '843 Patent.

Suzuki discloses a driving circuit for an LCD that seeks to improve the display of moving images on LCD devices. Suzuki at ¶¶ 8, 14, 18, 51. Like the ‘843 Patent, Suzuki recognizes that there is a time delay when applying a charge to a pixel of an LCD to alter its brightness level, which can result in blurring of displayed images. Id. at ¶ 4. Suzuki likewise describes the conventional overdrive technique, and posits that deficiencies in the conventional overdrive method render it insufficient to prevent blurring or “trails.” Id. at ¶¶ 5-7. To address the blurring issue, Suzuki describes a driving circuit that divides a frame period into a plurality of temporal subfields, and supplies data signal voltages (i.e., data impulses) to each of the liquid crystal cells of an LCD panel in each subfield of the frame period; the data signal voltages correspond to “overshoot” and “overdrive” values, both of which are overdriven pixel values. Id. at ¶¶ 11, 39, 42, 44, 46 & Fig. 2; Credelle Decl. at ¶¶ 64-67. Accordingly, multiple overdriven data impulses are applied to each pixel of the LCD panel within every frame period. Id.


Nitta was published on May 9, 2002, and is prior art to the ‘843 Patent under at least 35 U.S.C. § 102(b). All citations to Nitta herein refer to the certified English translation of the Japanese Patent Office publication, provided herewith as Exhibit Sony-1005. Nitta was not cited during the prosecution of the ‘843 Patent.
Nitta teaches an LCD device and driving method that “can display moving pictures with high picture quality in an active matrix liquid crystal display device.” Nitta at ¶ 1. Like the ‘843 Patent, Nitta acknowledges the “blurriness” issue when displaying moving pictures on LCD devices because “the response speed of the liquid crystal material is equal to or slower than the frame period of the display signal.” Id. at ¶¶ 2-3. Likewise, Nitta recognizes that prior attempts to address this issue have included “superimposing on the display signal a signal that emphasizes changes in the display signal,” but asserts that such methods are inadequate to accelerate the response speed of the liquid crystal material to one frame period or less. Id. at ¶¶ 4-5.

To solve this problem, Nitta discloses a liquid crystal control circuit that divides a frame period into a plurality of temporal subdivisions, referred to as “fields,” and applies a data voltage to every pixel of an LCD panel in each field. Id. at ¶ 9.

Specifically, in the first embodiment disclosed in Nitta, “one conventionally driven frame is divided into two fields, and driving is done at twice the speed.” Id. at ¶ 27.

In order to apply two data voltages within one frame period, the driving circuit of Nitta uses a liquid crystal timing controller to double the speed of the vertical and horizontal synchronization signals. Id. at ¶ 47 (“[T]he liquid crystal timing controller 104 supplies, to data driver 102 and scan driver 103, the liquid crystal synchronization signals FLM and CL1, CL3 in which VSYNC and HSYNC have accelerated two fold.”). Nitta’s driver circuit then applies the data voltages to the pixels of the LCD panel according to the doubled synchronization signals. Id. at ¶¶ 32 (“The liquid
crystal display device 100 of this embodiment . . . has . . . a data (signal) driver 102 that conveys to the signal lines of the TFT liquid crystal panel 101 voltages that correspond to the display data . . . .”), 49 (“according to CL1, gradation voltages corresponding to the OUT data are supplied to the signal lines”). In Nitta’s first embodiment, the data signal applied in the first field of the frame period corresponds to “corrected” or “conversion processed” data, and the data signal applied in the second field corresponds to the unchanged data for the frame period. Id. at ¶¶ 28, 37. As taught by Nitta, the “corrected” or “conversion processed” data is an example of overdriven data in the parlance of the ’843 Patent. Id. at ¶¶ 51-53 & Fig. 12; Credelle Decl. at ¶ 74. While the first embodiment of Nitta applies only one “conversion processed” data signal within a frame period, Nitta teaches that a frame period can be divided into three or more fields and “conversion processed” data signals applied in all but one of the fields, suggesting that multiple overdriven data voltages can be applied to each pixel of an LCD panel within one frame period. Nitta at ¶ 18 & claim 5. Nitta further teaches that the driving circuit of its first embodiment includes a data driver 102 that comprises a latch circuit (1) 83 and a latch circuit (2) 85. Id. at ¶ 43. The latch circuits serve to convert image data received in a serial stream of data into multiple parallel streams of data, so that corresponding data voltages can be applied to the pixels of the LCD panel line by line by a liquid crystal drive circuit 87 in synchronization with the multiplied horizontal synchronization signal CL1. Id. at ¶¶ 43-44; Credelle Decl. at ¶¶ 88-90.

Lee was filed on November 19, 2002, and published on November 20, 2003, and is prior art to the '843 Patent under at least 35 U.S.C. § 102(e). Lee was not cited during the prosecution of the '843 Patent.

Lee describes an LCD device in which dynamic capacitance compensation ("DCC") is performed. Lee at ¶ 2. Like the '843 Patent, Lee explains that because it takes time for a liquid crystal material to respond to an applied voltage, there is a delay in reaching a desired brightness level. Id. at ¶ 8. According to Lee, DCC addresses this issue by "process[ing] RGB data by comparing gray value for a pixel in a previous frame with gray value for a pixel in a current frame and adding a predetermined value larger than the difference between the gray values to the gray value of the previous frame," thus "minizi[ing] the time delay by applying a voltage larger than the predetermined voltage for a given gray to the pixel." Id. In other words, DCC is an example of an overdrive operation as described in the '843 Patent. See Credelle Decl. at ¶ 46. Lee illustrates several embodiments of circuits for performing DCC that include memory controllers for directing the operation of frame memories used for storing and outputting current and delayed frame data. Lee at Figs. 1, 2, 6, 8, 12.


Jinda was filed on August 2, 2001 and published on April 18, 2002, and is prior art to the '843 Patent under at least 35 U.S.C. § 102(b). Jinda was cited, but not discussed,
during the prosecution of the ‘843 Patent. Jinda discloses a driving circuit and method for an LCD device for improving the display quality of moving images. Jinda at ¶ 1. Like the ‘843 Patent, Jinda states that LCD devices have a disadvantage in displaying moving images compared to CRT devices due to the slow response speed of liquid crystals with respect to changes in transmittance. Id. at ¶ 2. Jinda also recognizes that prior attempts to address this problem included “superimposing a difference component by comparison with the previous image signal” (i.e., the overdrive method), but states that such methods were insufficient to allow a liquid crystal element to reach a desired transmittance level within one frame period. Id. at ¶¶ 4, 6.

To solve this issue, Jinda discloses an LCD device and driving method wherein a plurality of overdriven data signal voltages (i.e., data impulses) are applied to the pixels of an LCD panel within one vertical synchronization interval (i.e., a frame period). Id. at ¶¶ 8-10, 37-38.¹ Like the ‘843 Patent, image data is stored in memory to create

¹ A “vertical synchronization interval” as used in Jinda is a frame period. Credelle Decl. at ¶¶ 95-97. As shown in Fig. 2 of Jinda, image data is read into a “frame memory” in one vertical synchronization interval. Jinda at ¶¶ 37-38. The image data read in during the period of one vertical synchronization interval includes image data for each pixel of an LCD device. Jinda at ¶¶ 8-9; Credelle Decl. at ¶¶ 95-96. A frame is a complete screen or picture; accordingly, a vertical synchronization interval as described in Jinda is a frame period. Credelle Decl. at ¶ 97.
delayed frame data, and the value of the overdriven data voltages to be applied to the LCD panel are determined based on comparing the delayed frame data and current frame data. Id. at ¶¶ 37-38.

C. Statutory Grounds for Challenge

Cancelation of claims 1-3 is requested on the following grounds:

A. Claims 1 and 2 are invalid under 35 U.S.C. § 103 as being obvious over Suzuki in view of Nitta and Lee.

B. Claims 1 and 3 are invalid under 35 U.S.C. § 103 as being obvious over Jinda in view of Nitta and Lee.

D. Claim Construction

Generally, the claim terms should be given their broadest reasonable construction in view of the specification, and should be construed in accordance with their ordinary meaning. One specific term is discussed below.

1. “blur clear converter”

Claim 1 of the ‘843 patent recites “a blur clear converter for receiving frame data every frame period, each frame data comprising a plurality of pixel data and each pixel data corresponding to a pixel, the blur clear converter delaying current frame data to generate delayed frame data and generating a plurality of overdriven pixel data within every frame period for each pixel.” This language invokes 35 U.S.C. § 112(6), because “blur clear converter” is a coined term that is not recognized as a noun connoting structure, and does not connote sufficiently definite structure to a person of ordinary
skill in the art (“POSA”). See Credelle Decl. at ¶ 32; Mass. Inst. of Tech. v. A bacus Software, 462 F.3d 1344, 1353 (Fed. Cir. 2006); Lighting World, Inc. v. Birchwood Lighting, Inc., 382 F.3d 1354, 1360 (Fed. Cir. 2004) (“What is important is whether the term is one that is understood to describe structure, as opposed to a term that is simply a nonce word or a verbal construct that is not recognized as the name of structure and is simply a substitute for the term ‘means for.’”).

A means-plus-function limitation is construed by identifying the claimed function, and then determining the corresponding structure that is clearly linked to the function. See Medtronic, Inc. v. Advanced Cardiovascular Sys., 248 F.3d 1303, 1311 (Fed. Cir. 2001) (“Structure disclosed in the specification is ‘corresponding’ structure only if the specification or prosecution history clearly links or associates that structure to the function recited in the claim.”) (quoting B. Braun M ed., Inc. v. A bbott L abs., 124 F.3d 1419, 1424 (Fed. Cir. 1997)). The claimed functions for the “blur clear converter,” as recited in claim 1 of the ‘843 patent, are (1) “receiving frame data every frame period,” (2) “delaying current frame data to generate delayed frame data,” and (3) “generating a plurality of overdriven pixel data within every frame period for each pixel.” Credelle Decl. at ¶ 33.

The ‘843 patent discloses two embodiments of the “blur clear converter.” In the first embodiment, shown in Fig. 7, the structure clearly linked to the functions of (1) “receiving frame data every frame period” and (2) “delaying current frame data to generate delayed frame data” is a first image memory 44 controlled by a first memory
controller 48. ‘843 Patent at 4:44-55 & Fig. 7; Credelle Decl. at ¶ 34. The first image memory 44 receives frame data every frame period, and “[t]he first image memory 44 is controlled by the first memory controller 48 to delay current pixel data Gm for a frame period to generate delayed pixel data Gm-1.” ‘843 Patent at 4:49-53 & Fig. 7. In the first embodiment, the structure clearly linked to the function of (3) “generating a plurality of overdriven pixel data within every frame period for each pixel” is processing circuit 42, 2 which “generates a plurality of overdriven pixel data GN according to the current pixel data Gm and the delayed pixel data Gm-1.” Id. at 4:53-55 & Fig. 7; Credelle Decl. at ¶ 34. Therefore, the corresponding structure associated with the “blur clear converter” of claim 1 may comprise a memory and memory controller, which receive frame data every frame period and generate delayed pixel data, and a processing circuit for generating a plurality of overdriven pixel data according to the current pixel data and the delayed pixel data, and equivalents thereof.

A second embodiment of the “blur clear converter” is shown in Fig. 8, and is not further discussed herein. ‘843 Patent at 4:64-5:22.

IV. How the Challenged Claims Are Unpatentable (37 C.F.R. §42.104(b)(4)-(5))

2 While the ‘843 patent generally discloses a “processing circuit 42” for generating a plurality of overdriven pixel data, it does not sufficiently disclose any corresponding structure or algorithm for performing that function. See Aristocrat Techs. Australia Pty Ltd. v. Int’l Game Tech., 521 F.3d 1328, 1334-38 (Fed. Cir. 2008).
The challenged claims are invalid for the reasons discussed below.

**A. Claims 1-2 Would Have Been Obvious Over Suzuki in View of Nitta and Lee**

The crux of the alleged invention of independent claim 1 of the ’843 Patent is a driving circuit that generates multiple overdriven pixel data for each pixel of an LCD panel within every frame period according to received frame data, and that applies multiple data impulses to each of the pixels of the LCD panel within one frame period, with the data impulses corresponding to the overdriven pixel data. ’843 Patent at 1:8-12, 5:45-55 & claim 1. The remaining elements recited in claim 1 are nothing more than conventional LCD components. Id., claim 1; Credelle Decl. at ¶ 50.

As described in detail below, at least Suzuki expressly discloses the crux of claim 1. Suzuki at ¶¶ 9, 38, 40, 52-54. Suzuki also discloses an LCD panel but does not expressly describe its structure. Nitta describes the structural elements of a conventional LCD panel. Nitta at ¶ 32 & Fig. 3. Suzuki further describes an LCD driving circuit including a frame memory for generating and outputting delayed frame data, but does not expressly describe the controller required to operate the frame memory. Suzuki at ¶¶ 9, 38, 40. Lee describes a conventional LCD driving circuit for performing overdrive operations, and illustrates the memory controller for directing the operation of the frame memories. Lee at ¶¶ 2, 8, 11-12, 49, 52 & Figs. 1, 6. Thus, Suzuki in view of Nitta and Lee disclose every element of claim 1, and thus renders this claim obvious. And, as described below, Suzuki in view of Nitta and Lee also
renders dependent claim 2 obvious.

1. Claim 1

For the reasons set forth below, the combination of Suzuki, Nitta, and Lee renders claim 1 obvious, and thus invalid under 35 U.S.C. § 103.

i. A driving circuit for driving an LCD panel,

Suzuki teaches a “display control device of a liquid crystal panel for controlling display data to be displayed on the liquid crystal panel,” in which a timing control unit “outputs driving signals according to the received display data.” Suzuki at ¶¶ 2, 10. Thus, Suzuki discloses the preamble of claim 1. Likewise, Nitta teaches “a liquid crystal display device drive method” for a LCD device that has “a signal driver circuit.” Nitta at ¶ 1, 9. As such, Nitta also discloses the preamble of claim 1. Lee similarly teaches a “liquid crystal display” including a “gate driver” and a “source driver,” disclosing the preamble of claim 1. Lee at ¶¶ 2, 17.

ii. the LCD panel comprising

Although claim 1 purports to recite a “driving circuit” for an LCD panel, the claim also sets forth elements directed to the LCD panel itself. Specifically, according to claim 1, the LCD panel to be driven by the “driving circuit” comprises scan lines, data lines, and pixels, and is nothing more than a conventional LCD panel that was well known to a POSA. See Credelle Decl. at ¶¶ 50-54; Sony-1009 at 34. Indeed, in its preliminary response to a pending petition for inter partes review of the ‘843 Patent filed by a third party, the Patent Owner admitted that “[a] conventional LCD panel
includes a source driver connected to data lines arranged in a first direction, a gate driver connected to scan lines arranged in a second direction, and a matrix of pixels arranged at the intersection of each scan line and data line.” IPR2015-00021, Paper 9 at 3 (P.T.A.B. Jan. 20, 2015). Suzuki discloses a conventional LCD panel. See Suzuki at ¶¶ 38, 47, Fig. 1 (element 20).

Nitta discloses the details of a common TFT LCD panel. Nitta at ¶ 32 & Fig. 3. A POSA of LCD driving circuitry would have combined the conventional LCD panel of Nitta and the driving circuit of Suzuki, because both Suzuki and Nitta are directed to the same recognized problem in the field of LCD devices, blurring in the display of motion pictures caused by the slow response time of liquid crystal cells. See III.B.1, supra; Suzuki at ¶ 4; III.B.2, supra; Nitta at ¶¶ 2-3. Further, a POSA would also combine the teachings of Nitta and Suzuki because they both address the same problem in a similar way: they both apply multiple data signals to each pixel of an LCD device during every frame period to accelerate the liquid crystal response speed. See III.B.1, III.B.2, supra; Suzuki at ¶¶ 11, 39, 42, 44, 46; Nitta at Abstract, ¶¶ 27-28, 32, 37, 47, 49, 50-51; Credelle Decl. at ¶¶ 84-86. Thus, a POSA would have combined their teachings. See KSR Int'l Co. v. Teleflex Inc., 550 U.S. 398, 420 (2007) (“Under the correct analysis, any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed.”); see also Thomson Licensing SA S v. Int'l Trade Comm'n, 527 Fed. Appx. 884, 889 (Fed. Cir. 2013) (holding a POSA would have been
motivated to combine references that both “relate to LCD panel manufacturing and the formation of spacers” and “share the common goal of providing spacing elements that do not disturb the orientation or alignment of liquid crystal molecules”); Belden Techs. Inc. v. Superior Essex Commc’ns, 802 F. Supp. 2d 555, 572 (D. Del. 2011) (“It is prima facie obvious to combine two compositions each of which is taught by the prior art to be useful for the same purpose, in order to form a third composition which is used for the very same purpose.”) (quoting In re Kerkhoven, 626 F.2d 846, 850 (C.C.P.A. 1980)).

Each element of the claimed LCD panel is addressed below.

a. a plurality of scan lines;

Suzuki discloses a “gate driver” (18), but does not expressly describe gate or scan lines. Suzuki at ¶¶ 38 & Fig. 1. However, it was understood by a POSA that LCD panels typically comprised a plurality of scan lines. Credelle Decl. at ¶ 50-51; Sony-1009 at 34; Sony-1017 at ¶¶ 34-36 & Fig. 5. Moreover, Nitta explicitly teaches an LCD “that has a liquid crystal panel that has . . . multiple scan lines.” Nitta at ¶¶ 9, 32 & Fig. 3. Thus, to the extent that Suzuki does not explicitly describe an LCD panel having a plurality of scan lines, a POSA would have combined the driving circuit of Suzuki and the conventional LCD panel of Nitta (having a plurality of scan lines), as discussed above. Credelle Decl. at ¶¶ 84-86. Accordingly, the combination of Suzuki and Nitta discloses an LCD panel having a plurality of scan lines.

b. a plurality of data lines;
Suzuki discloses a liquid crystal display device that includes a “source driver” (16), but does not expressly describe data lines. Suzuki at ¶ 38 & Fig. 1. However, it was understood by a POSA that LCD panels typically comprised a plurality of data lines. See Credelle Decl. at ¶¶ 50-51; Sony-1009 at 34; Sony-1017 at ¶¶ 34-36 & Fig. 5. Further, Nitta explicitly teaches an LCD “that has a liquid crystal panel that has multiple signal [i.e., data] lines.” Nitta at ¶¶ 9, 32 & Fig. 3 (shown as vertical lines connecting the signal driver 102 to the pixels); Credelle Decl. at ¶¶ 78-79. The ‘843 Patent states that data impulses or voltages are applied to the pixels of the LCD panel via the corresponding data line. ‘843 Patent at 2:29-31, 3:47-51. Nitta likewise teaches that “display voltage that corresponds to the liquid crystal display data” is applied via signal lines. Nitta at ¶ 9. The signal lines taught by Nitta are thus the data lines recited in the claims of the ‘843 patent. Credelle Decl. at ¶¶ 78-79. As such, to the extent that Suzuki does not teach an LCD panel having a plurality of data lines, a POSA would have combined the conventional LCD panel of Nitta (having a plurality of data lines) with the driving circuit disclosed by Suzuki, as discussed above. Credelle Decl. at ¶¶ 84-86. Therefore, the combination of Suzuki and Nitta discloses an LCD panel having a plurality of data lines.

c. and a plurality of pixels . . .

Suzuki discloses an LCD panel (20) having “a plurality of pixels P which are formed in a matrix,” and that the pixels of the LCD panel comprise liquid crystal cells. Suzuki at ¶¶ 4, 47 & Fig. 1 (elements P). Suzuki does not specify that the pixels are
connected to corresponding scan and data lines, nor does Suzuki explicitly state that
the pixels include a switching device. However, a POSA at the time of the alleged
invention of the ‘843 Patent would have known that LCD panels were commonly
composed of a matrix of pixels comprising TFTs (Thin-Film Transistors), which
functioned as a switching device, and that the TFTs were connected to corresponding
scan lines, data lines, and liquid crystal elements. See Credelle Decl. at ¶¶ 50-54; Sony-
1008 at 18; Sony-1009 at 27, 34; Sony-1017 at ¶¶ 34-36 & Fig. 5. Additionally, Fig. 3
of Nitta (reproduced below) teaches an LCD device including a “TFT liquid crystal
panel 101, a data (signal) driver 102 that conveys to the signal lines of the TFT liquid
crystal panel 101 voltages that correspond to the display data, [and] scan drivers 103-1
and 103-2 that convey to the gate lines of the TFT liquid crystal panel 101 voltages
that correspond to the scan signals.” Nitta at ¶ 32. Fig. 3 of Nitta shows that the LCD
panel comprises a plurality of pixels located at the intersections of the data lines and
scan lines.

![Nitta, Fig. 3 (annotations added in red)](image)

While Nitta does not explicitly state that the TFTs act as the switching device for
each pixel of the LCD panel, it was known by a POSA that transistors function as
switches, and that TFTs in particular were used as switching devices for the pixels of
LCD panels. See Credelle Decl. at ¶¶ 52-54; Sony-1008 at 18; Sony-1009 at 27. Each of the liquid crystals of the TFT liquid crystal panel 101 responds to “a signal voltage corresponding to the display data . . . supplied to the signal line” and “a gate write pulse . . . supplied to scan lines.” Nitta at ¶¶ 50-51. As such, the LCD panel described in Nitta includes a plurality of pixels, with each pixel comprising a switching device (TFT) connected to a corresponding signal line (i.e., data line), scan line, and liquid crystal device. Credelle Decl. at ¶¶ 52-54, 72, 78-79. Thus, to the extent Suzuki does not explicitly show an LCD panel comprising a plurality of pixels, with each pixel including a switching element, a POSA would have combined the conventional LCD panel of Nitta with the driving circuit of Suzuki, as discussed above. Credelle Decl. at ¶¶ 84-86. Therefore, the combination of Suzuki and Nitta discloses an LCD panel having “a plurality of pixels, each pixel being connected to a corresponding scan line and a corresponding data line, and each pixel comprising a liquid crystal device and a switching device connected to the corresponding scan line, the corresponding data line, and the liquid crystal device.”

iii. the driving circuit comprising:

As described in detail below, the combination of Suzuki, Nitta, and Lee renders the recited driving circuit obvious.

a. a blur clear converter for . . . ;

Fig. 1 (reproduced below) shows the structure of the blur clear converter taught by Suzuki. The details of how Suzuki teaches the required functions and corresponding
structure of this mean-plus-function limitation are discussed below.

![Suzuki, Fig. 1 (annotations added in color)](image)

1. for receiving frame data . . .

As discussed above, for its first embodiment of the blur clear converter, the '843 patent clearly links first image memory 44 to the function of “receiving frame data every frame period, each frame data comprising a plurality of pixel data and each pixel data corresponding to a pixel.” See III.D, supra. Suzuki discloses both the function and the required structure for performing that function. Specifically, Suzuki teaches a driving circuit including a data memory unit 12a of frame memory 12 (i.e., image memory) that “stores image data to be supplied correspondingly to each single frame period.” Suzuki at ¶¶ 9, 38, 40 & Fig. 1. Suzuki further discloses that the driving circuit includes a data comparison unit 30 that compares the value of the image data of the newly received frame data with the value of the previous frame data “on each pixel of the liquid crystal panel.” Id. As such, Suzuki discloses a data memory unit of a frame memory (i.e., image memory) for “receiving frame data every frame period, each frame data comprising a plurality of pixel data and each pixel data corresponding to a pixel.”
2. delaying current frame data to generate delayed frame data

As discussed above, for its first embodiment of the blur clear converter, the ‘843 patent clearly links the first image memory 44 and the first memory controller 48 to the function of “delaying current frame data to generate delayed frame data.” See III.D, supra. Suzuki discloses that the data memory unit 12a of frame memory 12 (i.e., image memory) stores “image data of a frame immediately preceding.” Suzuki at ¶¶ 9, 40 & Fig. 1. Thus, the data memory unit 12a described in Suzuki generates delayed frame data by storing the image data of the preceding frame, just as the “blur clear converter” recited in the ‘843 patent generates delayed frame data by storing data for a preceding frame period in an image memory. ‘843 Patent at 4:49-53. While Suzuki does not expressly separate the data unit 12a or frame memory 12 into a memory and corresponding memory controller, a POSA would have known that memory controllers were routinely used to control the operation of memory units, particularly for addressing, reading and writing. Credelle Decl. at ¶¶ 57-61; Sony-1008 at 238-240; Sony-1010 at 186-188; Sony-1011 at 1261. Furthermore, Lee explicitly discloses a memory controller that controls a frame memory to generate delayed frame data. Fig. 1 of Lee (reproduced below) illustrates a prior art circuit that includes a memory controller 12 and frame memories 13 and 14, in which frame memory 14 stores previous frame data under the control of memory controller 12, thus generating delayed frame data. Lee at ¶¶ 11-12. Fig. 6 of Lee (reproduced below) illustrates an embodiment of the driving circuit claimed by Lee that includes a memory controller.
661 and frame memories 671 and 672, in which frame memory 672 stores previous frame data under the control of memory controller 661, thus generating delayed frame data. Lee at ¶¶ 49, 52.

To the extent Suzuki does not disclose a memory controller that controls the data memory unit 12a, a POSA would have combined the memory controller of Lee and the driving circuit of Suzuki, as both references address the known issue of slow liquid crystal response time using the overdrive technique, and both references disclose storing preceding frame data in a memory to implement the overdrive technique. See KSR, 550 U.S. at 420; Thomson, 527 Fed. Appx. at 889; Belden, 802 F. Supp. 2d at 572; Credelle Decl. at ¶ 92. Therefore, the combination of Suzuki and Lee discloses both the function of “delaying current frame data to generate delayed frame data” and the corresponding structure for performing the function (image memory and memory controller).

3. generating a plurality of overdriven pixel data . . .

Finally, as discussed above in Section III.D, for its first embodiment of the blur clear converter, the ‘843 patent clearly links a processing circuit 42 to the function of
“generating a plurality of overdriven pixel data within every frame period for every pixel.” As shown in Fig. 1 (reproduced above), Suzuki teaches a data conversion part 10 that generates multiple overdriven pixel data for each pixel in each frame period using the delayed frame data stored in the data memory unit 12a. “The data conversion part 10 is formed as an ASIC (Application Specific IC),” and thus constitutes a processing circuit. Suzuki at ¶ 40. Fig. 2 of Suzuki (reproduced below) “shows how a single pixel (liquid crystal cell) of the liquid crystal panel is written with data in the liquid crystal display device of the first embodiment.” Suzuki at ¶ 52.

![Suzuki, Fig. 2 (annotations added in red)](image)

As shown in Fig. 2 of Suzuki, a first “overshoot” voltage (a) is applied to the pixel during the first subfield of the frame period. This first voltage (a) is “higher than the target value” for the frame. Id. at ¶ 53. Then, during the second subfield of the frame period, a second “overdrive” voltage (c) is applied. The second voltage (c) is “slightly lower than the target applied voltage according to the target display data.” Id. at ¶ 54.  

3 Note that “the applied voltage VS is inverted in polarity upon each subfield scan . . . . For this reason, the applied voltage Vs has target values (+) and target values (-).” Suzuki at ¶ 52.
The '843 Patent states that overdriving “means applying a higher or a lower data impulse to the pixel electrode to accelerate the reaction speed of the liquid crystal molecules, so that the pixel can reach the predetermined gray level in a predetermined frame period.” '843 Patent at 2:2-5. As shown in Fig. 2, because the first voltage (a) and the second voltage (b) are applied during the same frame period (e.g., FL1), the transmittance value of the pixel reaches the target transmittance value within that frame period. Suzuki at ¶¶ 53-54. Thus, the first voltage (a), which is higher than the target value, and the second voltage (c), which is slightly lower than the target value, are both examples of “overdriven” voltages. See Credelle Decl. at ¶¶ 64-67.

While Fig. 2 of Suzuki shows that two overdriven data voltages are generated and applied for a single pixel, Suzuki’s teaches that two overdriven data voltages are generated for each pixel of the LCD panel. To accomplish this, Suzuki discloses a data conversion part 10 which includes a data comparison unit 30 that “determines, on each pixel of the liquid crystal panel, a difference between image data supplied anew and image data of a frame immediately preceding and stored in the data memory unit.” Suzuki at ¶¶ 9, 38, 40 & Fig. 1. The data conversion part 10 also includes an operational unit 32 which determines two overdriven pixel data for each pixel based on the difference between the current image data and the image data of the preceding frame, as determined by the data comparison unit. Id. at ¶¶ 11, 40-44.

Suzuki teaches that the operational unit 32 includes a first operational unit 32a that determines an “overshoot value” OSD for the first subfield SF1 of a frame period. Id.
at ¶ 42. The operational unit 32 also includes a second operational unit 32b that determines an “overdrive value” ODD for the second subfield SF2 of a frame period. Id. at ¶¶ 43-44. As discussed above, both of these modified voltage values OSD and ODD are examples of “overdriven signals” as that term is used in the ’843 Patent. Id. at ¶¶ 6, 11, 15, 41-44. Suzuki teaches that, in accordance with its first embodiment, “an overshoot operation and an overdrive operation are performed in a single frame period so that each pixel is changed to the transmittance corresponding to the image data,” and, “[c]onsequently, moving image data can be displayed at constant hues with improved display properties of moving images.” Id. at ¶¶ 64-67. Thus, Suzuki teaches the function of “generating a plurality of overdriven pixel data within every frame period for each pixel,” and the corresponding “processing circuit” for performing the function (data conversion part 10).

b. a source driver for generating a plurality of data impulses . . .

As an initial matter, the recitation of “scan line” in the above element appears to have been a draftsman’s error. The ’843 patent states that “scan voltages are applied to the scan lines [] to turn on the switching devices [], and the data voltages are applied to the data lines [] . . . .” ’843 patent at 3:47-49. This statement comports with the understanding of a POSA regarding the operation of LCD devices. Credelle Decl. at ¶ 62; Sony-1009 at 34. A POSA would therefore understand the reference to “scan line” in the element above as a typographical error meant to reference “data line” instead. Credelle Decl. at ¶ 62.
Suzuki teaches a source driver that generates a plurality of data impulses VS for each pixel of an LCD panel in each frame period according to the plurality of overdriven pixel data generated by the operational unit. Suzuki at ¶¶ 53-54. Fig. 1 of Suzuki shows a first embodiment of the disclosed driving circuit that includes a source driver 16. “The source driver 16 generates . . . the applied voltages VS to be supplied to pixels P (liquid crystal cells) of the liquid crystal panel.” Id. at ¶ 47. In Suzuki’s first embodiment, a frame period is divided into two subfields, and an applied voltage VS is applied to each pixel of the LCD display in each subfield. The source driver 16 applies a voltage VS, which corresponds to overdriven pixel data OSD, to each pixel of the LCD panel in the first subfield SF1. Id. at ¶ 53. Then, the source driver 16 applies a second voltage VS, which corresponds to overdriven pixel data ODD, to each pixel of the LCD panel in the second subfield SF2. Id. at ¶ 54. Thus, the source driver generates two data impulses for each pixel in each frame period according to the overdriven pixel data determined by the operational unit. See Section IV.A.1.iii.a.3, supra. These data impulses are applied within one frame period to control the transmission rate of the liquid crystal device of each pixel (“so that the time integral of the actual transmittance and the time integral of the target value of the transmittance become equal”). Suzuki at ¶¶ 52-58 & Fig. 2. Fig. 2 of Suzuki (reproduced below) “shows how a single pixel (liquid crystal cell) of the liquid crystal panel is written with data in the liquid crystal display device of the first embodiment.”. Id. at ¶ 52. As shown in Fig. 2, a voltage VS greater than the target value is applied during the first
subfield SF1 of the frame period FL1, and a voltage VS slightly lower than the target value is applied during the second subfield SF2 of that same frame period, so that the transmittance of each pixel reaches the transmittance target value within one frame period. Id. at ¶¶ 64-67. Both of these voltages are examples of “overdriven” voltages, as that term is used in the ’843 Patent. Credelle Decl. at ¶¶ 64-67; ’843 Patent at 4:49-53.

While Suzuki does not explicitly state that the data impulses are applied to the pixels of the LCD panel via the corresponding data lines, a POSA would have known that data voltages were typically applied to pixels via corresponding data lines. Credelle Decl. at ¶¶ 48-49; Sony-1009 at 34; Sony-1017 at ¶ 35. Moreover, to the extent Suzuki does not explicitly disclose that the data impulses are applied to the pixels of the LCD panel via corresponding data lines, Nitta explicitly teaches a source driver that conveys a plurality of data impulses to the pixels of an LCD panel via corresponding data lines. See IV.A.1.ii.b, supra; Nitta at ¶ 9. As shown in Fig. 3 (reproduced below), Nitta teaches a source driver (signal (data) driver 102) that generates a plurality of data impulses (“voltages that correspond to the display data”) and conveys them, in one frame period, to the pixels of the LCD panel via the data lines (the vertical lines connecting signal driver 102 to the pixels). Nitta at ¶¶ 9, 32 & Fig. 3; Credelle Decl. at ¶¶ 78, 80. More specifically, as shown in Fig. 8 (reproduced below), the liquid crystal driver circuit 87 of the source driver 102 produces (generates) the data impulses based on the display data. Nitta at ¶¶ 43-44 & Fig. 8. Fig.
4 of Nitta illustrates the operation of Nitta’s first embodiment and shows that each line of the LCD panel is scanned twice in a single frame period so that two data impulses are applied. Nitta at ¶¶ 38-39 & Fig. 4. Nitta further teaches that the pixels of the LCD comprise a liquid crystal device, and that the liquid crystals respond to data voltages (i.e., data impulses) applied via data lines. See IV.A.1.ii.c, supra; Nitta at ¶¶ 32, 50-51; Credelle Decl. at ¶¶ 78-79. Thus, Nitta teaches a source driver that applies two data impulses to the liquid crystal device of a pixel via a corresponding data line within a single frame period.

Both Suzuki and Nitta are directed to the same recognized problem in the field of LCD devices. See IV.A.1.ii, supra. Also, both Suzuki and Nitta address the problem in a similar manner, by applying multiple data impulses to the pixels of an LCD panel within a single frame period. See IV.A.1.ii, supra. Further, Nitta teaches that a frame period can be divided into three or more fields, and an overdriven data impulse applied in all but one of the fields, thus suggesting that multiple overdriven data impulses can be applied within a single frame period as in the driving circuit taught by Suzuki. Nitta at ¶ 18 & claim 5. Therefore, a POSA at the time of the purported invention of the ’843 Patent would have combined the use of a source driver which applies multiple data impulses to a liquid crystal device via data lines within one frame period, as disclosed in Nitta, with the driving circuit of Suzuki. See KSR, 550 U.S. at 420; Thomson, 527 Fed. Appx. at 889; Belden, 802 F. Supp. 2d at 572; Credelle Decl. at
¶¶ 84-86. As such, the combination of Suzuki and Nitta discloses a source driver for “generating a plurality of data impulses to each pixel according to the plurality of overdriven pixel data generated by the blur clear converter and applying the data impulses to the liquid crystal device of the pixel via the [data] line connected to the pixel within one frame period in order to control transmission rate of the liquid crystal device.”

Suzuki, Fig. 2             Nitta, Fig. 3              Nitta, Fig. 8
(annotations in red)     (annotations in color)           (highlighting added)

c. a gate driver for applying a scan line voltage . . . .

Suzuki teaches that the driving circuit for the LCD display includes a gate driver. Suzuki at ¶ 38. Further, Suzuki teaches that the gate driver 18 “generates gate signals GT [i.e., scan line voltage] for selecting pixels P of the liquid crystal panel in synchronization with the timing signals TIM.” Id. at ¶ 47. Fig. 1 of Suzuki shows an embodiment of the driving circuit taught by Suzuki, including the gate driver 18 and gate signals GT. A POSA at the time of the alleged invention of the ‘843 Patent would have known that LCD panels commonly comprised a matrix of pixels including TFTs, with the TFTs functioning as switching devices for the pixels of the LCD display. Credelle D ecl. at ¶¶ 50-54; Sony-1008 at 18; Sony-1009 at 27, 34; Sony-
Further, a POSA understood that the purpose of a gate driver was to apply voltage to a row of TFTs via the corresponding scan line, thus activating the row of TFTs so that data voltages could be applied to the liquid crystal cells of the pixels. Credelle Decl. at ¶¶ 55-56; Sony-1008 at 18; Sony-1009 at 34; Sony-1017 at ¶¶ 35-36 & Fig. 5. As such, Suzuki discloses a gate driver for applying a scan line voltage to the switch device of a pixel so that a data impulse can be applied to the liquid crystal device of the pixel.

Additionally, as shown in Fig. 3 of Nitta (reproduced below), Nitta teaches “scan drivers” (i.e., gate drivers) 103-1, 103-2 that “convey to the gate lines [scan lines 1, 2, etc.] of the TFT liquid crystal panel . . . voltages that correspond to the scan signals.” Nitta at ¶¶ 9, 32; Credelle at ¶¶ 76-77. Nitta further teaches that the pixels of the LCD comprise a liquid crystal device connected to the switching device, and that the liquid crystals respond to applied data voltages (i.e., data impulses). Id. at ¶¶ 9, 32, 50- 51. The timing diagram of Fig. 4 shows how each scan line of the TFT LCD matrix is scanned twice for each frame. Nitta at ¶ 39. As noted above, a POSA understood that TFTs were used as switching devices for the pixels of an LCD panel, and that scan signals and gate drivers (as disclosed in Nitta) were used to activate the TFTs of pixels so that data impulses could be applied to the liquid crystal cell of the pixel. See Credelle Decl. at ¶¶ 50-56; Sony-1008 at 18; Sony-1009 at 27, 34; Sony-1017 at ¶¶ 34-36 & Fig. 5. The ‘843 Patent likewise states that a gate driver applies scan voltages to scan lines to turn on the switching devices of pixels on an LCD panel. ‘843
Thus, “scan driver” as used by Nitta is just another name for a “gate driver” as recited in the claims of the ‘843 patent. See Credelle Decl. at ¶¶ 76-77. Accordingly, to the extent Suzuki does not explicitly describe applying a scan line voltage to the switching device of a pixel via a corresponding data line so that a data impulse is applied to the liquid crystal device, a POSA at the time of the purported invention of the ‘843 Patent would have combined the driving circuit of Suzuki and the use of the conventional gate driver and TFTs of Nitta, as both references are directed to the same known problem in the field of LCD devices. See KSR, 550 U.S. at 420; Thomson, 527 Fed. Appx. at 889; Belden, 802 F. Supp. 2d at 572; Credelle Decl. at ¶¶ 76-77, 84-86. Accordingly, the combination of Suzuki and Nitta discloses “a gate driver for applying a scan line voltage to the switch device of the pixel so that the data impulses can be applied to the liquid crystal device of the pixel.”

2. Claim 2

Claim 2 depends from claim 1, and adds limitations relating to the structure of the “blur clear converter” recited in claim 1. As discussed above, the combination of Suzuki, Nitta, and Lee renders claim 1 obvious. See IV.A.1, supra. Suzuki in view of
Nitta and Lee render claim 2 obvious in two ways as set forth below.

   i. Analysis I:

        a. The driving circuit of claim 1 wherein the blur clear converter further comprises:

Suzuki’s third embodiment, in view of Lee, discloses the additional limitations that claim 2 adds to claim 1. Although the analysis above in connection with claim 1 references Suzuki’s first embodiment, that analysis applies equally to Suzuki’s third embodiment. As discussed above, in Suzuki’s first embodiment, a single frame period is divided into two subfields SF1 and SF2 within which overdriven pixel data OSD and ODD are respectively applied to each pixel during every frame period. Suzuki at ¶¶ 39, 52-58. In Suzuki’s third embodiment, however, a single frame period is divided into three subfields SF1, SF2, and SF3, and three overdriven pixel data OSD1 (corresponding to OSD of the first embodiment), OSD2, and ODD (corresponding to ODD of the first embodiment) are respectively applied to each pixel during every frame period. Id. at ¶¶ 81-82. Fig. 6 of Suzuki (reproduced below) shows the structure of the driving circuit of Suzuki’s third embodiment. Suzuki at ¶ 80. “In this embodiment, a single frame period is divided into three subfields SF1, SF2, and SF3. . . . For this reason, the data conversion part 10 and timing control unit 14 of the first embodiment are replaced with a data conversion part 10C and a timing control unit 14C. The rest of the configuration is almost the same as in the first embodiment.” Id. at ¶ 81. Thus, in Fig. 6 of Suzuki, “[t]he same elements as those described in the first embodiment will be designated by identical reference numbers,” and “[d]etailed
description thereof will be omitted.” Id. at ¶ 80; compare Suzuki, Fig. 6, with Suzuki, Fig. 1. In Suzuki’s third embodiment, “[t]he first operational unit 36a, second operational unit 36b, and third operational unit 36c are circuits corresponding to the first operational unit 32a, second operational unit 32b, and third operational unit 32c of the first embodiment, respectively,” and generate overdriven pixel data for the first subfield SF1 and third subfield SF3. Id. at ¶ 82. The fourth and fifth operational units 36d and 36e are added to the operational unit 36 of Suzuki’s third embodiment, and generate overdriven pixel data for the second subfield SF2. Id. at ¶ 82-83.

As discussed above, Suzuki’s third embodiment teaches a driving circuit in which “a single frame period is divided into three subfields SF1, SF2, and SF3.” Suzuki at ¶ 81. Thus, the rate of the subfields is three times the frame rate. See Suzuki, Fig. 7. In each of the three subfields, a data impulse is generated and applied to each of the pixels of an LCD panel. Id. at ¶¶ 82-89 & Fig. 7. The data impulses correspond to overdriven pixel data generated by a data conversion part 10C; a first operational unit 36a determines the overdriven value OSD1 for the first subfield “simultaneously with
the start of the subfield SF1.” Id. at ¶¶ 42, 82. Likewise, a fifth operational unit 36e restores an overdriven value OSD2 for the second subfield “in synchronization with the start of the subfield SF2”, and a third operational 36c unit restores an overdriven value ODD for the third subfield “simultaneously with the start of” the third subfield SF3. Id. at ¶¶ 44, 82, 84.

It would have been obvious to a POSA to include a multiplier in the data conversion part 10C for multiplying the control signal of the incoming frame data, so that the functions of the operational units 36a, 36c, and 36e can be synchronized with the subfields SF1, SF2, and SF3 as required by Suzuki. See Credelle Decl. at ¶¶ 68-71; Suzuki at ¶¶ 81-82, 84. Indeed, a multiplied control signal is required to synchronize the functions of the operational units with the timing of the three subfields SF1, SF2, and SF3, particularly since the operational units 36a, 36c, and 36e operate “simultaneously with the start” of subfields SF1, SF2, and SF3; the driving circuit of Suzuki’s third embodiment could not function otherwise. See Credelle Decl. at ¶¶ 68-71; Suzuki at ¶¶ 42, 44, 82, 84. Accordingly, the driving circuit disclosed by Suzuki renders “a multiplier for multiplying the frequency of a control signal to generate a multiplied signal” obvious.

   c. a first image memory for delaying the pixel data for a frame period;

As set forth above with respect to claim 1, Suzuki discloses a first embodiment of a driving circuit that generates delayed frame data by storing it in data memory unit 12a for a frame period. See IV.A.1.iii.a.2, supra; Suzuki at ¶¶ 9, 40. Suzuki’s third
embodiment likewise includes a data memory unit 12a that generates delayed frame data by storing it for a frame period. Id. at ¶¶ 80-81 & Fig. 6 (element 12a). Therefore, the data memory unit 12a of Suzuki’s third embodiment is an image memory for delaying pixel data for a frame period, and Suzuki discloses this element.

d. a processing circuit for generating the plurality of overdriven pixel data . . .;

As discussed above with respect to claim 1, Suzuki’s first embodiment discloses a data conversion circuit 10 (processing circuit) that generates two overdriven pixel data for each pixel in every frame period based on the difference between current image data and image data for a preceding frame (delayed pixel data) that is stored in the data memory unit. See IV.A.1.iii.a.3, supra; Suzuki at ¶¶ 6, 9, 11, 15, 38, 40-44, 52-54, 64-67 & Figs. 1, 2. Suzuki’s third embodiment discloses a data conversion circuit 10C (processing circuit) that functions in the same manner as the data conversion circuit 10 of the first embodiment, but generates three overdriven pixel data for each pixel in every frame period instead of two overdriven pixel data. Suzuki at ¶¶ 80-86 & Figs. 6, 7. The data conversion circuit 10C “is formed as an ASIC (Application Specific IC).” Suzuki at ¶ 82. Thus, Suzuki’s third embodiment also discloses a “processing circuit for generating the plurality of overdriven pixel data according to the pixel data and the pixel data delayed by the first image memory”.

e. a second image memory for storing the overdriven pixel data;

Suzuki’s third embodiment teaches a frame memory comprising a second image memory for storing a plurality of overdriven pixel data generated by a data conversion
circuit. Suzuki at ¶ 83-84. Specifically, as shown in Fig. 6 (reproduced above), Suzuki teaches a driving circuit comprising a frame memory 12 that includes a first memory unit 12b and second memory unit 12c. Id. at ¶ 80 & Fig. 6.

Suzuki’s third embodiment divides a single frame period into three temporal subfields, and generates overdriven pixel data for each pixel of an LCD panel in each of the subfields. See IV.A.2.i.b, IV.A.2.i.d, supra; Suzuki at ¶¶ 6, 9, 11, 15, 80-86 & Fig. 7. The overdriven pixel data is generated by an operational unit 36, which comprises five operational units. Suzuki at ¶ 82 & Fig. 6. “[T]he fourth operational unit 36d initially determines an overshoot value pixel by pixel” to be displayed in the second temporal subfield of the input frame period, then “determines a difference between the overdrive value determined and the target value corresponding to image data supplied anew, and writes the difference determined to a second memory unit 12c of the frame memory 12 as difference data.” Suzuki at ¶ 83. Similarly, the second operational unit 36b “initially determines an overdrive value pixel by pixel” to be displayed in the third temporal subfield of the input frame period, then “determines differences between the overdrive values determined and the target values corresponding to image data supplied anew, and writes the differences determined to a first memory unit 12b of the frame memory 12 as difference data.” Suzuki at ¶¶ 43-44, 80, 82 & Fig. 6. Thus, the first memory unit 12b and second memory unit 12c constitute a second image memory for storing the plurality of overdriven pixel data generated by the operational units 36b and 36d in the form of difference data.
Accordingly, Suzuki discloses this element.

f. a memory controller for controlling the second image memory . . . .

As discussed above, Suzuki teaches a third embodiment of a driving circuit comprising a second image memory (first memory unit 12b and second memory unit 12c) for storing a plurality of overdriven pixel data, but does not explicitly describe the details of the second image memory as including a memory controller. See IV.A.2.i.e, supra; Suzuki at ¶¶ 43-44, 80, 82-83 & Fig. 6. However, as discussed above, fifth operational unit 32e and third operational unit 36c “restore” overdrive values OSD2 and ODD for use in the subfields SF2 and SF3, respectively, in synchronization with the start of subfields SF2 and SF3; the overdrive values are “restored” from image data (overdriven pixel data in the form of difference data) stored in second memory unit 12c and first memory unit 12b. See IV.A.2.i.b, supra; Suzuki at ¶¶ 43-44, 80, 82-84 & Fig. 6. Accordingly, each of the second memory unit 12c and first memory 12b (second image memory) outputs its respective overdriven pixel data (in the form of difference signals) in synchronization with the start of subfields SF2 and SF3. As discussed above with respect to claim 1, the use of memory controllers to direct the operation of memory devices was well known by a POSA, and Lee teaches a memory controller for directing the operation of frame memories used in an overdrive circuit. See IV.A.1.iii.a.2, supra; Lee at ¶¶ 11-12, 49, 52 & Figs. 1, 6; Credelle Decl. at ¶¶ 57-61; Sony-1008 at 238-240; Sony-1010 at 186-188; Sony-1011
Therefore, to the extent Suzuki does not describe a controller for controlling the operation of the second image memory, a POSA would have combined the memory controller taught by Lee with the driving circuit taught by Suzuki, as both references address the known issue of slow liquid crystal response time using the overdrive technique, and both references disclose storing image data in memory to implement the overdrive technique. See KSR, 550 U.S. at 420; Thomson, 527 Fed. Appx. at 889; Belden, 802 F. Supp. 2d at 572; Credelle Decl. at ¶ 92.

Further, as set forth above, Suzuki renders the use of a multiplier for generating a multiplied control signal obvious. See IV.A.2.i.b, supra. It would have been obvious to a POSA that the memory controller for the second image memory would control the second image memory according to the multiplied control signal, as such would be necessary to have the second image memory output the overdriven pixel data in synchronization with the three temporal subfields of the input frame period, as required by Suzuki. Credelle Decl. at ¶¶ 68-71. Additionally, Suzuki teaches that its third embodiment comprises a source driver 16 (the same as included in Suzuki’s first embodiment) that generates a plurality of overdriven data impulses for each pixel of an LCD display within a single frame period according to the overdriven pixel data generated by data conversion part 10C and stored in the second image memory. Suzuki at ¶¶ 80, 82-89 & Fig. 7. Specifically, the driving circuit of Suzuki’s third embodiment includes a timing control unit 14C that “successively receives the display data OSD1, OSD2, and ODD from the first operational unit 36a, fifth operational
unit 36e, and third operational unit 36c, respectively, and outputs these display data OSD1, OSD2, and ODD to the source driver 16 as driving signals DRV.” Suzuki at ¶ 85. The source driver 16 generates applied voltages VS corresponding to the display data for each pixel in each of the three subfields SF1, SF2, and SF3, as shown in Fig. 7 (reproduced below). Suzuki at ¶¶ 86-89 & Fig. 7. Accordingly, the source driver 16 generates a plurality of data impulses to each pixel of the LCD panel in accordance with the overdriven pixel data generated by the data conversion part 10C and output by the second image memory. Thus, the combination of Suzuki and Lee discloses “a memory controller for controlling the second image memory according to the multiplied signal to output the plurality of overdriven pixel data to any pixel so that the source driver generates the data impulses to each pixel within one frame period according to the overdriven pixel data output by the second image memory.”

Suzuki, Fig. 7 (annotations added in red)

ii. Analysis II

a. The driving circuit of claim 1 wherein the blur clear converter further comprises:

The combination of Suzuki and Nitta discloses the additional limitations that claim 2 adds to claim 1, thus rendering claim 2 obvious.
Nitta discloses a multiplier for multiplying a frequency of a control signal to generate a multiplied signal. In particular, Nitta teaches a first embodiment of an LCD device including a liquid crystal timing controller 104 that receives display control signals 120, including horizontal synchronization signal HSYNC, from a display signal source via line 120 of Fig. 3. Nitta at ¶¶ 32-35 & Fig. 3. Nitta further discloses that the liquid crystal timing controller 104 provides a scan clock signal CL3, which is twice the speed of HSYNC, to scan drivers 103-1 and 103-2, and provides a data horizontal clock CL1, which is also twice the speed of HSYNC, to data driver 102 (via line 107). Nitta at ¶¶ 34, 38 & Figs. 3, 8. As such, the liquid crystal timing controller 104 disclosed in Nitta includes “a multiplier for multiplying a frequency of a control signal to generate a multiplied signal,” and Nitta discloses this element.

It would have been obvious to use a multiplier as disclosed in Nitta in the driving circuit taught by Suzuki. As discussed above with respect to claim 1, Suzuki and Nitta address the same known problem in the field of LCD devices. See IV.A.1.ii, supra. Also, like Nitta, Suzuki applies two data impulses to the pixels of an LCD panel in every frame period, thus doubling the frequency at which data impulses are applied relative to the input frequency. See IV.A.1.iii.b-c, supra; Suzuki at ¶¶ 6, 9, 11, 15, 52-54, 58, 64; Nitta at ¶¶ 27, 39 & Fig. 4. Thus, a POSA would have combined the teachings of Suzuki with the teachings of Nitta. See KSR, 550 U.S. at 420; Thomson, 527 Fed. Appx. at 889; Belden, 802 F. Supp. 2d at 572; Credelle Decl. at ¶¶ 87-91.
c. a first image memory for delaying the pixel data for a frame period;

As set forth above, Suzuki discloses a first image memory (data memory unit 12a) that generates delayed pixel data by storing it for a frame period. See IV.A.1.iii.a.2, supra; Suzuki at ¶¶ 9, 40 & Fig. 1.

d. a processing circuit for generating the plurality of overdriven pixel data . . . ;

As discussed above, Suzuki discloses a processing circuit (data conversion unit 10) for “generating the plurality of overdriven pixel data according to the pixel data and the pixel data delayed by the first image memory.” See IV.A.1.iii.a.3, IV.A.2.i.d, supra; Suzuki at ¶¶ 6, 9, 11, 15, 38, 40-44, 52-54, 64-67 & Figs. 1, 2.

e. a second image memory . . . ; a memory controller for . . . the second image memory . . . .

Additionally, Nitta discloses a driving circuit that includes a second image memory for storing and outputting overdriven pixel data such that a plurality of overdriven data impulses are applied to each pixel of an LCD panel within a single frame period. Nitta at ¶¶ 9, 43-44 & Figs. 1, 8. As discussed above, Nitta discloses a driving circuit for an LCD device that includes a data driver 102. See IV.A.1.iii.b, supra; Nitta at ¶¶ 9, 32 & Fig. 3. The data driver 102 stores data for display on an LCD panel in a latch circuit (1) 83 and subsequently in latch circuit (2) 85; the liquid crystal driving circuit 87 of the data driver 102 produces data impulses (“liquid crystal drive voltage”) corresponding to the data stored in the latch circuits (1) and (2), such that two data impulses are applied to the pixels of the LCD panel within a single frame period. Nitta
Figure 8 of Nitta (reproduced below) illustrates the data driver, and shows the latch circuits (1) and (2) that receive data for display. A POSA at the time of the purported invention of the ‘843 Patent would have understood that a latch circuit is a memory device. See Credelle Decl. at ¶ 87; Sony-1012 at 607-08.

Nitta further teaches a memory controller that controls the latch circuits (1) and (2) to output the plurality of overdriven pixel data such that the liquid crystal driving circuit 87 (i.e., the source driver) generates corresponding data impulses to the pixels of the LCD panel within a single frame period. Specifically, as shown in Fig. 3 (reproduced below), Nitta teaches a liquid crystal timing controller 104 that supplies a set of data driver drive signals 107 to the data driver 102. Nitta at ¶ 34. The drive signals 107 include clock signal CL1, “which is a signal of twice the speed of the horizontal synchronization signal HSYNC of the input.” Id. at ¶ 38. As shown in Fig. 8, the data driver 102 includes a latch circuit (2) 85 which receives clock signal CL1 from the liquid crystal timing controller 104. Id. at ¶ 43. The data driver 102 also includes a multi-selection shift register, which produces a selection signal 82 such that “the display data 106 (DATA) that is input while synchronized to the transmission clock CL2 that is emitted from the liquid crystal timing controller 104 is captured, in

4 While the latch circuits of Nitta are located in the data driver, and claim 2 requires that the blur clear converter comprise the second image memory, claim 2 does not require complete separation between the blur clear converter and source driver.
sequence, in the latch circuit (1) 83.” Id. The latch circuit (2) 85 latches the display data that is held in the latch circuit (1) 83 in accordance with the clock signal CL1, so that the display data “is synchronized to the data horizontal synchronization signal CL1.” Id. at ¶ 44. The liquid crystal drive circuit 87 generates and applies data impulses (“drive voltage”) “based on the latch data 86 of the latch (2) 85, driving the liquid crystal panel 101.” Id. As discussed above with respect to claim 1, the data driver 102 generates a plurality of data impulses for each pixel in every frame period. See IV.A.1.iii.b, supra; Nitta at ¶¶ 9, 32, 38-39, 43-44, & Figs. 3, 8. Thus, the liquid crystal timing controller 104 is the memory controller for the second image memory (latch circuits (1) 83 and (2) 85), and generates clock signals CL1 and CL2 to control the second image memory to output the plurality of pixel data so that the liquid crystal drive circuit 87 generates a plurality of corresponding data impulses to each pixel of the LCD panel in a single frame period.

As discussed above with respect to claim 1, a POSA would have combined the driving circuit of Suzuki with the source driver of Nitta, at least because both references are addressed to the same known issue in the field of LCD technology. See KSR, 550 U.S. at 420; Thomson, 527 Fed. Appx. at 889; Belden, 802 F. Supp. 2d at 572. Furthermore, it would have been desirable to combine (more specifically) the latch circuits (1) 83 and (2) 85 of Nitta with the driving circuit of Suzuki, as these latch circuits synchronize the display data so that the display data can be converted to appropriate data impulses at the appropriate time in each frame period, line by line for
each frame. Credelle Decl. at ¶¶ 87-91. As such, the combination of Suzuki and Nitta discloses a “second image memory for storing the overdriven pixel data” and “a memory controller for controlling the second image memory according to the multiplied signal to output the plurality of overdriven pixel data to any pixel so that the source driver generates the data impulses to each pixel within one frame period according to the overdriven pixel data output by the second image memory.”

B. Claims 1 and 3 Would Have Been Obvious Over Jinda in View of Nitta and Lee

As described in detail below, at least Jinda expressly discloses the crux of claim 1. Jinda at ¶ 10, 37-38, 41. Jinda also discloses an LCD panel but does not expressly describe its structure. Nitta, however, describes the structural elements of a conventional LCD panel. Nitta at ¶ 32 & Fig. 3. Jinda further describes an LCD driving circuit including frame memories for generating and outputting delayed frame data, but does not expressly describe the controller required to operate the frame memories. Lee describes a conventional LCD driving circuit for performing overdrive operations, and illustrates the memory controller for directing the operation of the frame memories. Thus, the combination of Suzuki, Nitta, and Lee discloses every
element of claim 1, and therefore renders this claim invalid as obvious. And, as
described in detail below, the combination of Suzuki, Nitta, and Lee also renders
dependent claim 3 obvious.

1. Claim 1

As set forth in detail below, the combination of Jinda, Nitta, and Lee renders
claim 1 obvious. Therefore, claim 1 is invalid under 35 U.S.C. § 103.

i. A driving circuit for driving an LCD panel,

Jinda teaches “a liquid crystal display device driving method for driving a liquid
crystal display device,” and illustrates a drive circuit for carrying out the method. Jinda
at ¶¶ 8, 19 & Fig. 1. Accordingly, Jinda discloses the preamble of claim 1. As
discussed above with respect to ground 1, Nitta and Lee likewise disclose the
preamble of claim 1. See IV.A.1.i, supra; Nitta at ¶¶ 1, 9; Lee at ¶¶ 2, 17.

ii. the LCD panel comprising:

As set forth above with respect to ground 1, claim 1 purports to recite a
“driving circuit” for an LCD panel, but also sets forth elements directed to the LCD
panel itself. These elements comprise nothing more than a conventional LCD panel
that was well known to a POSA. See Credelle Decl. at ¶¶ 50-51; Sony-1009 at 34. Jinda
discloses a method and circuit for driving an LCD device having a plurality of pixels.
Jinda at ¶¶ 8, 38. As discussed above with respect to ground 1, Nitta discloses the
details of a conventional LCD panel. See IV.A.1.ii, supra. A POSA would have
combined the driving circuit of Jinda and the conventional LCD panel of Nitta, as
both references are directed to the same recognized issue in the field of LCD devices: blurring in the display of motion pictures caused by the slow response time of liquid crystal cells. See III.B.2, III.B.4, supra; Nitta at ¶¶ 2-3; Jinda at ¶ 2. Further, both Jinda and Nitta address the problem in a similar way: by applying multiple data voltages to each pixel during every frame period to accelerate the liquid crystal response speed. Jinda at ¶¶ 8-10, 37-38; Nitta at Abstract, ¶¶ 27-28, 32, 37, 47, 49-51. Therefore, a POSA would have combined their teachings. See KSR, 550 U.S. at 420; Thomson, 527 Fed. Appx. at 889; Belden, 802 F. Supp. 2d at 572; Credelle Decl. at ¶¶ 101-102. Each of the elements of the recited LCD panel is addressed below.

a. a plurality of scan lines;

As discussed above with respect to ground 1, Nitta discloses an LCD panel having a plurality of scan lines. See IV.A.1.i.a, supra; Nitta at ¶¶ 9, 32 & Fig. 3. To the extent Jinda does not explicitly describe the details of the LCD panel, a POSA would have combined the driving circuit of Jinda with the conventional LCD panel of Nitta, as both references are directed to the same recognized issue in the field of LCD technology, and address the problem in a similar manner as discussed above. See IV.A.1.i, supra; KSR, 550 U.S. at 420; Thomson, 527 Fed. Appx. at 889; Belden, 802 F. Supp. 2d at 572; Credelle Decl. at ¶¶ 101-102. Thus, the combination of Jinda and Nitta discloses an LCD panel having a plurality of scan lines.

b. a plurality of data lines;

As set forth with respect to ground 1 above, Nitta discloses an LCD panel
having a plurality of data lines. See IV.A.1.ii.b, supra; Nitta at ¶¶ 9, 32 & Fig. 3. To the extent Jinda does not explicitly describe the details of the LCD panel, a POSA would have combined the driving circuit of Jinda with the LCD panel of Nitta, as both references are directed to the same recognized issue in the field of LCD technology, and address the problem in a similar manner. See KSR, 550 U.S. at 420; Thomson, 527 Fed. Appx. at 889; Belden, 802 F. Supp. 2d at 572; Credelle Decl. at ¶¶ 101-102. Thus, the combination of Jinda and Nitta discloses an LCD panel having a plurality of data lines.

c. and a plurality of pixels . . .

As discussed above with respect to ground 1, Nitta discloses an LCD panel having a plurality of pixels comprising a switching device connected to corresponding scan lines, data lines, and liquid crystal elements. See IV.A.1.ii.c, supra; Nitta at ¶¶ 9, 32, 50-51 & Fig. 3. To the extent Jinda does not explicitly describe the details of the LCD panel, a POSA would have combined the driving circuit of Jinda with the conventional LCD panel of Nitta, as both references are directed to the same recognized issue in the field of LCD technology, and address the problem in a similar manner as discussed above. See IV.B.1.ii, supra; KSR, 550 U.S. at 420; Thomson, 527 Fed. Appx. at 889; Belden, 802 F. Supp. 2d at 572; Credelle Decl. at ¶¶ 101-102. Thus, the combination of Jinda and Nitta discloses an LCD panel having “a plurality of pixels, each pixel being connected to a corresponding scan line and a corresponding data line, and each pixel comprising a liquid crystal device and a switching device
connected to the corresponding scan line, the corresponding data line, and the liquid crystal device.”

iii. the driving circuit comprising:

As described in detail below, the combination of Jinda, Nitta, and Lee renders obvious the recited driving circuit.

a. a blur clear converter for . . .;

Fig. 1 of Jinda (reproduced below) shows the structure of the blur clear converter taught by Jinda. The details of how Jinda teaches the functions and corresponding structure of this means-plus-function limitation are discussed below.

Jinda, Fig. 1 (annotations added in color)

1. for receiving frame data every frame period . . .

As discussed above in Section III.D, for its first embodiment of the blur clear converter, the ‘843 Patent clearly links first image memory 44 to the function of “receiving frame data every frame period, each frame data comprising a plurality of pixel data and each pixel data corresponding to a pixel.” Jinda discloses both the function, and the required structure for performing that function. Specifically, Jinda teaches a driving circuit that receives frame data every frame period from a video source, and stores the frame data “as input image signals to a first frame memory 1, a second frame memory 2 and a third frame memory 3.” Jinda at ¶ 36. Jinda also
teaches that the input image data is “to be written into each pixel of the liquid crystal display device.” Id. at ¶¶ 8, 36. Accordingly, Jinda discloses three frame memories (i.e., image memories) for “receiving frame data every frame period, each frame data comprising a plurality of pixel data and each pixel data corresponding to a pixel.”

2. delaying current frame data to generate delayed frame data . . .

As discussed above in Section III.D, for its first embodiment of the blur clear converter, the '843 Patent clearly links the first image memory 44 and the first memory controller 48 to the function of “delaying current frame data to generate delayed frame data.” Jinda discloses that the three frame memories (i.e., image memories) 1, 2, and 3 each receive and store frame data for a frame period once in every three frame periods. Jinda at ¶ 37. Figs. 2 and 3 of Jinda (reproduced below) illustrate the operation of the frame memories:

For example, as shown in Fig. 2, frame data A is written to the first frame memory 1 during a first frame period (vertical synchronization interval), and, as shown in Fig. 3, frame data A is read from the first frame memory 1 during the two subsequent frame periods. Therefore, as shown in Figs. 2 and 3 of Jinda, the driving circuit disclosed by Jinda generates delayed frame data by storing frame data for the two frame periods in
two of the three frame memories, while the current frame data is written into the third
frame memory. While Jinda does not explicitly show that the frame memories include
both a memory and a corresponding controller, a POSA at the time of the alleged
invention of the '843 Patent would have known that memory controllers were
conventionally used to control the operation of memories in LCD driving circuitry.
See Credelle Decl. at ¶¶ 57-61; Sony-1008 at 238-240; Sony-1010 at 186-188; Sony-
1011 at 1261. Moreover, as set forth above with respect to ground 1, Lee explicitly
discloses memory controllers that control frame memories to generate delayed frame
data. See IV.A.1.iii.a.2, supra; Lee at ¶¶ 11-12, 49, 52 & Figs. 1, 6. To the extent Jinda
does not disclose a memory controller that controls the frame memories 1, 2, and 3 to
generate delayed frame data, a POSA would have combined the memory controller of
Lee and the driving circuit of Jinda, as both references disclose storing preceding
frame data in a frame memory to implement the overdrive technique. See KSR, 550
U.S. at 420; Thomson, 527 Fed. Appx. at 889; Belden, 802 F. Supp. 2d at 572; Credelle
Decl. at ¶ 106. As such, the combination of Jinda and Lee discloses both the function
of “delaying current frame data to generate delayed frame data” and the
corresponding structure for performing the function (image memory and memory
controller).

3. generating a plurality of overdriven pixel data . . .

Finally, as discussed above in Section III.D, the first embodiment of the blur clear
converter set forth in the '843 Patent clearly links a processing circuit 42 to the
function of “generating a plurality of overdriven pixel data within every frame period for every pixel.” Jinda’s first embodiment teaches an arithmetic unit 4 that generates two overdriven pixel data within every frame period for every pixel based on a comparison of the image data for the current frame to be displayed and for the preceding frame that is stored in two of the three frame memories 1, 2, and 3. A block diagram of this first embodiment is shown in Fig. 1 (reproduced above).

The arithmetic unit 4 receives image data read out from two of the three frame memories in any given frame period. Jinda at ¶ 37. The arithmetic unit 4 then determines overdriven pixel data for each pixel of the LCD device using a “look-up table” that provides an overdriven value according to the current pixel data and the delayed pixel data obtained from the frame memories. Id. at ¶¶ 38, 44. An example of the look-up table is shown in Fig. 4 of Jinda (reproduced below). Id. at ¶ 39. As shown in Fig. 4 of Jinda, the arithmetic unit’s look-up table returns a data value higher than the current frame’s data value when the data value of the previous frame was lower, and returns a data value lower than the current frame’s data value when the data value of the previous frame was higher. Id. at ¶ 40. Thus, the values returned by the look-up table are “overdriven pixel data” as described in the ’843 Patent. ‘843 Patent at 2:2-7. Fig. 5 of Jinda (reproduced below) illustrates the operation of Jinda’s first embodiment with respect to a single pixel.
In Fig. 5 of Jinda, “the reference character (a) represents a (target) data value to be written,” and “the reference character (b) represents the data value inputted from the arithmetic unit.” Jinda at ¶ 41. “[A]s shown in FIG. 5, the data value (b) of the value greater than the data value (a) to be written is inputted to the liquid crystal display device 5 repetitively two times in one vertical synchronization interval.” Id. The overdriven data value (b) generated by the arithmetic unit 4 is “supplied the plurality of times within one vertical synchronization interval and written into each pixel” of the LCD panel. Id. at ¶ 10. As shown in Fig. 5, the pixel reaches its target intensity (a) during one frame period as a result of applying the two data values (b). Id. at Fig. 5. Therefore, Jinda teaches an arithmetic unit 4 (processing circuit) for “generating a plurality of overdriven pixel data within every frame period for each pixel,” disclosing both the function and the corresponding structure (processing circuit) of this element.

b. a source driver for generating a plurality of data impulses . . .

As set forth above with respect to ground 1, the recitation of “scan line” appears to have been a draftsman’s error meant to reference a “data line” instead. See IV.A.1.iii.b, supra; Credelle Decl. at ¶ 62; Sony-1009 at 34. Jinda teaches that voltages corresponding to the plurality of overdriven pixel data generated by the arithmetic
unit 4 are “applied to the pixel electrode (not shown) of the desired pixel . . . .” Jinda at ¶ 38. A POSA at the time of the alleged invention would have known that data impulses were typically generated by a source or data driver and applied to the pixels of an LCD panel via corresponding data lines. See Credelle Decl. at ¶¶ 48-49; Sony-1009 at 34; Sony-1017 at ¶ 35.

Further, as discussed above with respect to ground 1, Nitta teaches a source driver 102 that generates a plurality of data impulses and conveys them, in one frame period, to the pixels of an LCD panel 101 via corresponding data lines. See IV.A.1.iii.b, supra; Nitta at ¶¶ 9, 32, 43-44 & Figs. 3, 8. Nitta further teaches that the pixels of the LCD comprise a liquid crystal device, and that the liquid crystals respond to applied data voltages (i.e., data impulses). See IV.A.1.ii.c, supra; Nitta at ¶¶ 32, 50-51. As discussed above, both Nitta and Jinda are directed to the same recognized problem in the field of LCD devices. See IV.B.1.ii, supra. In addition, both Jinda and Nitta address the problem in a similar manner, by applying multiple data impulses to the pixels of an LCD panel within a single frame period. See IV.B.1.ii, supra. Further, Nitta teaches that a frame period can be divided into three or more fields, and an overdriven data impulse applied in all but one of the fields, suggesting that multiple overdriven data impulses can be applied within a single frame period as in the driving circuit taught by Jinda. Nitta at ¶ 18 & claim 5. Accordingly, a POSA would have combined the driving circuit of Jinda and the source driver and data lines of Nitta. See KSR 550 U.S. at 420; Thomson, 527 Fed. Appx. at 889; Belden, 802 F. Supp. 2d at 572; Credelle Decl. at ¶¶
Therefore, the combination of Jinda and Nitta discloses a “source driver for generating a plurality of data impulses to each pixel according to the plurality of overdriven pixel data generated by the blur clear converter and applying the data impulses to the liquid crystal device of the pixel via the scan line connected to the pixel within one frame period in order to control transmission rate of the liquid crystal device.”

c. a gate driver for applying a scan line . . . .

Jinda teaches that data impulses are applied to the pixels of the LCD device, but does not describe this operation in detail. See IV.B.1.iii.a.1, supra; Jinda at ¶ 38. However, a POSA at the time of the alleged invention of the ‘843 Patent would have known that gate drivers were ordinarily used in conventional LCD panels to apply voltage to the switching device of a pixel in an active matrix LCD panel (commonly a TFT) so that a data impulse could be applied to the corresponding liquid crystal element. See Credelle D ecl. at ¶¶ 55-56; Sony-1008 at 18; Sony-1009 at 34; Sony-1017 at ¶¶ 35-36 & Fig. 5.

Moreover, as discussed above with respect to ground 1, Nitta teaches a gate driver that applies scan line voltage to the switching devices of the pixels of an LCD panel so that data impulses can be applied to the pixels, with each scan line of a TFT LCD matrix scanned twice in each frame period. See IV.A.1.iii.c, supra; Nitta at ¶¶ 32, 39 & Fig. 4; Credelle D ecl. at ¶¶ 76-77. Nitta also teaches that the pixels comprise a liquid crystal device connected to the switching device, and that the liquid crystals respond
to applied data voltages (i.e., data impulses). See IV.A.1.ii.c, supra; Nitta at ¶¶ 32, 50-51.

To the extent Jinda does not explicitly disclose a gate driver that applies a scan line voltage to the switch device of a pixel so that a data impulse is applied to the liquid crystal device of the pixel, a POSA would have combined the driving circuit taught by Jinda with the gate driver taught by Nitta, as both references are directed to the same known problem in the field of LCD technology and address the problem in a similar manner. KSR, 550 U.S. at 420; Thomson, 527 Fed. Appx. at 889; Belden, 802 F. Supp. 2d at 572; Credelle Decl. at ¶¶ 103-104. Therefore, the combination of Jinda and Nitta discloses “a gate driver for applying a scan line voltage to the switch device of the pixel so that the data impulses can be applied to the liquid crystal device of the pixel.”

2. Claim 3

i. The driving circuit of claim 1 wherein the blur clear converter further comprises:

As discussed above, the combination of Jinda, Nitta, and Lee renders claim 1 obvious. See IV.B.1, supra. Jinda, Nitta, and Lee further disclose the additional limitations that claim 3 adds to claim 1.

ii. a multiplier for multiplying a frequency of a control signal . . .;

As discussed above with respect to ground 1, Nitta discloses a multiplier for multiplying a frequency of a control signal to generate a multiplied signal. See IV.A.2.ii.b, supra; Nitta at ¶¶ 32-35, 38 & Figs. 3, 8. A POSA would have combined the multiplier disclosed in Nitta and the driving circuit and method disclosed by Jinda. Credelle Decl. at ¶ 105. As previously noted, both Jinda and Nitta are directed to the
same recognized problem in the field of LCD technology, and address the problem in a similar manner. See IV.B.1.ii, supra. Also, like Nitta, Jinda applies two data impulses to the pixels of an LCD panel in every frame period, thus doubling the frequency at which data impulse are applied relative to the input frequency. See IV.B.1.iii.b-c, supra; Jinda at ¶¶ 10, 37-41, 44 & Fig. 5; Nitta at ¶¶ 27, 39 & Fig. 4. Therefore, a POSA would have combined the teachings of Jinda and Nitta. See KSR, 550 U.S. at 420; Thomson, 527 Fed. Appx. at 889; Belden, 802 F. Supp. 2d at 572. Accordingly, the combination of Jinda and Nitta discloses a “multiplier for multiplying a frequency of a control signal to generate a multiplied signal.”

iii. a first image . . .; a second image memory . . .; a third image memory . . .;

As discussed above, Jinda discloses that its first embodiment comprises three frame memories. See IV.B.1.iii, supra. In any given frame period, one of the three frame memories is being written with new image data (temporarily storing pixel data), a second frame memory stores image data for the current frame (delayed data), and the remaining frame memory stores image data for a preceding frame (thus, delaying the frame data an additional frame period). See Jinda at ¶ 37 & Figs. 2, 3. For example, and as shown in Figs. 2 and 3 (reproduced below), during a third frame period (vertical synchronization period), frame data C is written to and temporarily stored in third frame memory 3, frame data B (the “previous” frame) is read from second frame memory 2 (delayed by two frame periods), and frame data A (the “current” frame) is read from third frame memory 1 (delayed by one frame period).
The three frame memories included in Jinda’s first embodiment are not connected in series such that the output of the third frame memory is input and stored in the second frame memory, and the output of the second frame memory is input and stored in the first frame memory. However, Jinda’s second embodiment teaches an alternative design in which two FIFO (First-In First-Out) memories are connected in series, such that the second FIFO memory receives the output of the first FIFO memory and delays it by one frame period. Jinda at ¶¶ 55, 57 (“the same image data as the image data outputted from the first FIFO memory 21 is outputted from the second FIFO memory 22 with a delay of one image period”). Fig. 10 of Jinda (reproduced below) illustrates this alternative arrangement.

It would have been obvious to a POSA that the three parallel frame memories used in Jinda’s first embodiment could be rearranged in a series arrangement (as suggested by Jinda’s alternative second embodiment) to achieve the arrangement recited in claim 3, without any change in function or result. See Credelle Decl. at ¶¶ 98-100; In re Yufa, 452 Fed. Appx. 998, 1001 (Fed. Cir. 2012) (affirming rejection of
claims as obvious in reexamination and stating patent claimed “nothing more than a reconfiguration of a known system); Nano-Second Tech. Co., Ltd. v. Dynaflex Int'l, 944 F. Supp. 2d 855, 863-864 (C.D. Cal. 2013) (“Although the [elements] of the #655 Patent are not arranged in the same manner as in the #311 Patent, they perform the same function, and achieve the same result . . . A person of ordinary skill in the art would be expected to consider and effectuate mere design changes . . . ”). The first frame memory would receive and temporarily store image data, the second image memory would delay the image data by a frame period, and the third image memory would delay the image data by an additional frame period, such that the arithmetic unit would determine overdriven values based on the image data output from the second image memory (delayed by one frame period) and the image data output from the third image memory (delayed by two frame periods), just as in Jinda’s first embodiment. See Jinda at ¶¶ 38-40 & Figs. 2, 3. The frame memories may constitute FIFO memories, as suggested by Fig. 10 of Jinda. Such an embodiment would constitute a mere design variation accomplished using known prior art elements for their recognized function, without any novel or unexpected results. See KSR, 550 U.S. at 417; Credelle Decl. at ¶ 100.

The driving circuit disclosed by Jinda accomplishes the same function as the driving circuit recited in claim 3 in the same manner: generating and applying a plurality of overdriven data impulses to each pixel of an LCD display within a single frame period. See IV.B.1, supra. As such, it would have been obvious that the frame
memories used in Jinda’s first embodiment could be connected in series as a design choice, particularly since Jinda itself discloses an alternative embodiment in which two FIFO memories are connected in series. See Credelle Decl. at ¶¶ 98-100; Jinda at ¶¶ 55, 57 & Fig. 10. Accordingly, the driving circuit disclosed by Jinda renders obvious a “a first image memory for receiving and temporarily storing the pixel data; a second image memory for delaying the pixel data stored and output by the first image memory for a frame period,” and “a third image memory for delaying the pixel data stored and output by the second image memory for a frame period.”

iv. a memory controller . . .;

As discussed above, Jinda does not explicitly describe a memory controller for managing the operation of the frame memories included in the disclosed driving circuit. See IV.B.1.iii.a.2, supra. However, a PO SA at the time of the purported invention of the ’843 Patent would have known that memory controllers were conventionally used to direct the operation of memory devices, particularly with respect to read, write, and address operations. See Credelle Decl. at ¶¶ 57-61; Sony-1009 at 238-240; Sony-1010 at 186-188; Sony-1011 at 1261. In addition, as discussed with respect to ground 1 above, Lee explicitly discloses a memory controller for directing the operation of frame memories in a driving circuit for performing overdrive operations. See IV.A.1.iii.a.2, supra; Lee at ¶¶ 11-12, 49, 52 & Figs. 1, 6. To the extent Jinda does not explicitly disclose a memory controller that directs the operation of the frame memories 1, 2, and 3, a PO SA would have combined the
driving circuit of Jinda and the memory controller of Lee to operate in accordance
with a multiplied signal (as discussed above), as both references address the known
issue of slow liquid crystal response time using the overdrive technique, and both
references disclose storing preceding frame data in a memory to implement the
overdrive technique. See KSR, 550 U.S. at 420; Thomson, 527 Fed. Appx. at 889; Belden,
802 F. Supp. 2d at 572; Credelle Decl. at ¶ 106. Therefore, the combination of Jinda
and Lee discloses “a memory controller for controlling the second image memory and
the third image memory according to the multiplied signal.”

v. a processing circuit . . .; and a comparing circuit . . . .

As discussed above with respect to claim 1, Jinda discloses an arithmetic unit 4
(processing circuit) that generates a plurality of overdriven pixel data by comparing
pixel data read out from two of the three frame memories 1, 2, and 3. See
IV.B.1.iii.a.3, supra; Jinda at ¶¶ 10, 37-39, 41 & Figs. 1, 4, 5. As shown in Figs. 2 and 3
of Jinda (reproduced below), the image data that is read out from the frame memories
to the arithmetic unit 4 consists of image data that is delayed for one frame period and
image data that is delayed for two frame periods. While frame memory 3 is written
with image data C, frame memories 1 and 2 read out image data A and B, respectively,
to the arithmetic unit 4. Image data A has been delayed two frame periods since it was
read into frame memory 1, while image data B has been delayed one frame period
since it was read into frame memory 2. Thus, the arithmetic unit 4 generates
overdriven pixel data by comparing pixel data (via the table shown in Figure 4) that
has been delayed two frame periods (i.e., image data output by the third image memory as recited in claim 3) and pixel data that has been delayed one frame period (i.e., image data output by the second image memory as recited in claim 3). Thus, the arithmetic unit 4 comprises both the “processing circuit” and “comparing circuit” recited in claim 3. Accordingly, Jinda discloses “a processing circuit for generating the plurality of overdriven pixel data according to the pixel data delayed and output by the second image memory and the third image memory,” and “a comparing circuit for comparing the pixel data delayed by the second image memory with the pixel data delayed by the third image memory in order to determine data values of the overdriven pixel data generated by the processing circuit.” Jinda at ¶¶ 38-40.

Jinda, Fig. 2 (annotations added in red)  Jinda, Fig. 3 (annotations added in red)

VI. Conclusion

In view of the foregoing, Petition requests that inter partes review of the ’843 Patent be instituted, and claims 1-3 be cancelled.

Dated: March 16, 2015

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Certificate of Service Under 37 C.F.R. § 42.6(e)(4)

I certify that I caused a true and correct copy of the foregoing Petition for Inter Partes Review of U.S. Patent No. 7,202,843, together with Petitioners’ Exhibits and Petitioner’s Powers of Attorney, to be served via EXPRESS MAIL® on the following:

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