UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MAXLINEAR, INC.
Petitioner

v.

CRESTA TECHNOLOGY CORPORATION
Patent Owner

CASE: IPR2015-00592
Patent 7,075,585

Title: Broadband Receiver having a Multistandard Channel Filter

PETITION FOR INTER PARTES REVIEW OF
U.S. PATENT NO. 7,075,585
UNDER 35 U.S.C. § 312 AND 37 C.F.R. § 42.100 ET SEQ.

Mail Stop PATENT BOARD
U.S. Patent Trial & Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
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**EXHIBIT LIST**

Exhibit 1101  U.S. Patent No. 7,075,585 (“the ‘585 patent”).


Exhibit 1104  U.S. Patent No. 6,643,502, titled “Multi-standard Reception,” to Van De Plassche et al. (“Van De Plassche” or “VDP”).


Exhibit 1110  U.S. Patent No. 5,278,872, titled “System and Circuit Architecture for Echo Cancellation and a Television Receiver Comprising Same,” to Greenberg (“Greenberg”).

Exhibit 1109  U.S. Patent No. 5,673,293, titled “Method and Apparatus for Demodulating QAM and VSB Signals,” to Scarpa et al. (“Scarpa”).

Exhibit 1111  IEEE 100: The Authoritative Dictionary of IEEE Standards
Terms, Seventh Edition

Exhibit 1112  Excerpts of the prosecution file history of the ‘792 patent.


Exhibit 1120  “Micronas Introduces First All CMOS Intermediate Frequency (IF) Chip To Handle Analog and Digital Broadcast Signals (0020),” November 21, 2000 (“Micronas’00”).


Exhibit 1122  W. Boie, “Broadcast Receiver Adapted for Analog and


Exhibit 1127 RF Microelectronics, Behzad Razavi, Publisher: Prentice Hall, 1997 (“Razavi’97”).


Exhibit 1132 CMOS Wireless Transceiver Design, Jan Crols and Michiel


Exhibit 1135  D. Ehrhardt and T. Benkner, wrote a paper published in the August 1993 issue of the IEEE Transactions on Consumer Electronics (“Ehrhardt’93”).

Petitioner hereby requests that the United States Patent and Trademark Office proceed with an *inter partes* review of claims 1–21 of U.S. Patent No. 7,075,585 (“the ’585 patent”) (Ex. 1101).

I. **COMPLIANCE WITH FORMAL REQUIREMENTS**

A. **Grounds for Standing (37 C.F.R. § 42.104(a))**

In accordance with 37 C.F.R. § 42.104(a), Petitioner certifies that the ’585 patent is available for *inter partes* review. Petitioner further certifies that Petitioner is not barred or estopped from requesting an *inter partes* review challenging the ’585 patent on the grounds identified in this Petition.

B. **Real Parties-In-Interest (37 C.F.R. § 42.8(b)(1))**

MaxLinear, Inc. (“Petitioner”) and Cresta Technology Corporation (“Patent Owner” or “Cresta Technology”) are the real parties-in-interest in this matter.

C. **Related Matters (37 C.F.R. § 42.8(b)(2))**

Patent Owner has filed two actions against Petitioner in which Patent Owner alleges that Petitioner infringes the ’585 patent: *Cresta Technology Corporation v. Maxlinear, Inc. et al.*, Case No. 1:14-cv-00079-RGA, filed on January 21, 2014, in the U.S. District Court for the District of Delaware (Complaint, Ex. 1102); and Investigation No. 337-TA-910, filed on January 28, 2014, in the International Trade Commission (“ITC”) (ITC Complaint, Ex. 1103). In both cases, Patent Owner also sued certain of Petitioner’s customers (e.g., Sharp Corporation and
In addition to these lawsuits, Petitioner and co-defendant/co-respondent, Silicon Laboratories, Inc. ("SiLabs") have filed the following petitions seeking *inter partes* review of the Cresta patents asserted in the ITC Complaint:

<table>
<thead>
<tr>
<th>Proceeding No.</th>
<th>Patent at Issue</th>
<th>Filing Date</th>
<th>Petitioner</th>
</tr>
</thead>
<tbody>
<tr>
<td>2014-00728</td>
<td>7,075,585</td>
<td>May 5, 2014</td>
<td>Silicon Laboratories</td>
</tr>
<tr>
<td>2014-00809</td>
<td>7,265,792</td>
<td>May 23, 2014</td>
<td>Silicon Laboratories</td>
</tr>
<tr>
<td>2015-00615</td>
<td>7,075,585</td>
<td>January 23, 2015</td>
<td>Silicon Laboratories</td>
</tr>
<tr>
<td>2015-00626</td>
<td>7,265,792</td>
<td>January 26, 2015</td>
<td>Silicon Laboratories</td>
</tr>
<tr>
<td>2015-00591</td>
<td>7,075,585</td>
<td>January 28, 2015</td>
<td>MaxLinear</td>
</tr>
<tr>
<td>2015-00592</td>
<td>7,075,585</td>
<td>January 28, 2015</td>
<td>MaxLinear</td>
</tr>
<tr>
<td>&quot;Petition&quot;</td>
<td>7,075,585</td>
<td>January 28, 2015</td>
<td>MaxLinear</td>
</tr>
<tr>
<td>2015-00593</td>
<td>7,265,792</td>
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<td>MaxLinear</td>
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<tr>
<td>2015-00594</td>
<td>7,265,792</td>
<td>January 28, 2015</td>
<td>MaxLinear</td>
</tr>
</tbody>
</table>

On October 24, 2014, the Board instituted review of claims 1-3, 5, 10, and 16-19 of the ’585 patent in IPR2014-00728.

**D. Counsel and Service Information (37 C.F.R. § 42.8(b)(3)-(4))**

Address all e-mails and telephone calls to lead and back up counsel (each associated with the above Customer Number), listed below:
<table>
<thead>
<tr>
<th><strong>Lead Counsel</strong></th>
<th><strong>Back-Up Counsel</strong></th>
</tr>
</thead>
</table>
| Name: Thomas J. Wimbiscus  
(Reg. No. 36,059)  
(twimbiscus@mcandrews-ip.com)  
Direct: 312-775-8109 | Name: Christopher C. Winslade  
(Reg. No. 36,308)  
(cwinslade@mcandrews-ip.com)  
Direct: 312-775-8108 |
| | Name: Gregory C. Schodde  
(Reg. No. 36,668)  
(gschodde@mcandrews-ip.com)  
Direct: 312-775-8117 |
| | Name: Scott P. McBride  
(Reg. No. 42,853)  
(smcbride@mcandrews-ip.com)  
Direct: 312-775-8131 |
| | Name: Ronald H. Spuhler  
(Reg. No. 52,245)  
(rspuhler@mcandrews-ip.com)  
Direct: 312-775-8210 |
| | Wayne H. Bradley  
(Reg. No. 39,916)  
(wbradley@mcandrews-ip.com)  
Direct: 312-775-8187 |

Address all communications to:

Thomas J. Wimbiscus  
Christopher C. Winslade  
Gregory C. Schodde  
Scott P. McBride  
Ronald H. Spuhler  
Wayne H. Bradley  
MCANDREWS HELD & MALLOY  
500 W. Madison, 34th Flr.  
Chicago, IL 60661  
Telephone: 312-775-8000 Facsimile: 312-775-8100
Please direct all correspondence regarding this proceeding to the lead counsel at the address listed above. Patent Owner also consents to electronic service by e-mail to MXL-IPR@mcandrews-ip.com.

The Patent Trial and Appeal Board is hereby authorized to charge any fees associated with this proceeding to Deposit Account 13-0017 (Customer ID 23446).

E. Statement of Precise Relief Requested

In accordance with 37 C.F.R. § 42.22, Petitioner respectfully requests cancellation of claims 1–21 of the ’585 patent.

II. REASONABLE LIKELIHOOD TO PREVAIL

This Petition, in accordance with 35 U.S.C. § 314(a), establishes a reasonable likelihood that Petitioner will prevail with respect to at least one of the claims challenged in this petition because the Petition provides evidence and supporting reasoning showing that all of the elements of each of claims 1–21 of the ’585 patent are unpatentable over the prior art.

III. IDENTIFICATION OF CHALLENGE

A. Prior Art Publications

Petitioner relies on the following prior art publications:

1. Van De Plassche et al., U.S. Patent No. 6,643,502, titled “Multi-standard Reception,” filed July 23, 1998 (Exhibit 1104) (“Van De Plassche” or “VDP”). VDP claims priority to PCT Application PCT/IB98/00676,


B. Identification of Challenge (37 C.F.R. § 42.104(b)) and Relief Requested (37 C.F.R. § 42.22(a)(1))

Petitioner challenges claims 1–21 (“the challenged claims”) of the ’585 patent. Petitioner requests IPR of Claims 1-21 on the grounds set forth in the table below, and requests that they be found unpatentable and be canceled. The Petition explains in detail the reasons why claims 1-21 are unpatentable under the relevant statutory grounds and includes an identification of where each element can be found in the cited prior art and the relevance of that prior art. Additional explanation and support for each ground of rejection is set forth in the Declaration of Dr. Hashemi. (Ex. 1113.)
<table>
<thead>
<tr>
<th>Grounds</th>
<th>‘585 patent Claims</th>
<th>Basis for Rejection</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ground 1</td>
<td>1, 2, 4, 5, 10 and 12-20</td>
<td>Obvious under 35 U.S.C. §103(a) over VDP in view of Ishikawa</td>
</tr>
<tr>
<td>Ground 2</td>
<td>3</td>
<td>Obvious under 35 U.S.C. §103(a) over VDP in view of Ishikawa and further in view of Malkemes</td>
</tr>
<tr>
<td>Ground 3</td>
<td>6, 7, 9 and 21</td>
<td>Obvious under 35 U.S.C. §103(a) over VDP in view of Ishikawa and further in view of Balaban</td>
</tr>
<tr>
<td>Ground 4</td>
<td>8</td>
<td>Obvious under 35 U.S.C. §103(a) over VDP in view of Ishikawa and further in view of Tsividis</td>
</tr>
<tr>
<td>Ground 5</td>
<td>11</td>
<td>Obvious under 35 U.S.C. §103(a) over VDP in view of Ishikawa and further in view of Greenberg</td>
</tr>
</tbody>
</table>

Grounds 1-5 in the Petition are not redundant with respect to the prosecution history, instituted IPR proceedings or co-pending IPR petitions.
1. **Grounds are Not Redundant of the Original Prosecution**

VDP, Malkemes and Balaban were admitted in the ’585 patent as being prior art. VDP was relied upon by the Examiner to initially reject claims 1, 2, 4, 5 and 10-20 of the ’585 patent during original prosecution of the ’585 patent. In particular, the Examiner identified all of the features of claims 1, 2, 4, 5 and 10-20 in VDP except for the limitations requiring a plurality of separate demodulators in independent claims 1 and 17.

VDP and Balaban were relied upon by the Examiner to initially reject claims 6, 7, 9 and 21. In particular, the Examiner identified all features of dependent claims 6, 7, 9 and 21 except for the aforementioned limitations in independent claims 1 and 17.

Despite allowance by the Examiner based on the plurality of demodulators feature of claims 1 and 17, this feature was well-known in the art prior at the time that the application for the ’585 patent was filed. It was well-known that each of the plurality of demodulators would receive a common input from a signal processor and operate according to a format, such as an analog or a digital format. (Ex. 1113, Hashemi’s Dec., ¶¶65-85.) Such knowledge is evidenced, for example, by the disclosure in Ishikawa, which was not reviewed by the Examiner. (Id.)

Grounds 1-5 in the Petition are better than the grounds for rejection in the original examination of the ’585 patent at least with respect to Ishikawa’s
disclosure of the plurality of separate demodulators for analog and digital formats. Ground 4 in the Petition is better than the grounds for rejection in the original examination of the ’585 patent at least with respect to Tsividis’ disclosure of the transconductance (gmC) filter function. Ground 5 in the Petition is better than the grounds for rejection in the original examination of the ’585 patent at least with respect to Greenberg’s disclosure of the FIR filters stored in a memory.

2. **Grounds are Not Redundant of Other Petitions for IPR**

**IPR2014-00728**

Silicon Labs’ petition for IPR2014-00728 sets for the following grounds:

**Ground 1:** Claims 1, 2, 5, and 16–19 are invalid under 35 U.S.C. § 102 as anticipated by Thomson (EP Application 0696854).

**Ground 2:** Claims 1, 2, 5, 10, 13 and 16 are invalid under 35 U.S.C. § 103 as obvious over Thomson in view of Harris (Olmstead et al., “A Digital Tuner for Wideband Receivers”).

**Ground 3:** Claims 1, 2, 5, and 16 are invalid under 35 U.S.C. § 103 as obvious over Thomson in view of TI App Note (“Implementation of FIR/IIR Filters with the TMS32010/TMS32020”).

**Ground 4:** Claims 1, 2, 5, 10, 13 and 16 are obvious over Thomson in view of the Admitted Prior Art or, in the alternative,
Thomson and Harris in further view of Admitted Prior Art.

**Ground 5**: Claim 3 is invalid under 35 U.S.C. § 103 as obvious over Thomson and Harris in further view of Kerth (USP 6,804,497).

**Ground 6**: Claims 13, 14, and 19 are invalid under 35 U.S.C. § 103 as obvious over Thomson and Harris in further view of Balaban

**IPR2015-00615**

Silicon Labs’ petition for IPR2015-00615 sets for the following grounds:

**Ground 1**: Claims 11 and 12 are invalid under 35 U.S.C. § 103 as obvious over Thomson, in view of Harris, and further in view of Grumman.

**Ground 2**: Claims 13, 15, and 20 are invalid under 35 U.S.C. § 103 as obvious over Thomson, in view of Harris, and further in view of Zenith.

**Ground 3**: Claim 14 is invalid under 35 U.S.C. § 103 as obvious over Thomson and Harris, in view of Zenith, and further in view of Birleson.

The challenged claims in the current Petition comprise claims 4, 6-9 and 21, which are not included in IPR2014-00728 or IPR2015-00615.
VDP as cited in the current Petition may be considered stronger than Thomson as cited in IPR2014-00728 and IPR2015-00615 with respect to the specific description of elements found in the ‘585 patent. For example, VDP labels input RF signals “Srf”; VDP labels the anti-alias filter “AAF”; and VDP labels the analog-to-digital converter “ADC.” Ishikawa may be considered stronger than Thomson with respect to Ishikawa’s illustration of the plurality of separate demodulators for analog and digital formats.

Grounds in the Petition are better, in some respects, than the grounds in the petition for IPR2014-00728 and IPR2015-00615 for at least the following reasons:

- VDP’s specific description of claim elements as cited in Grounds 1-5 and the Patent Office’s reliance on VDP during original prosecution;
- Ishikawa’s separate demodulators as cited in Grounds 1-5;
- Malkemes’s disclosure of a digital-to-analog converter that comprises digital and analog outputs and as cited in Ground 2 and the Patent Office’s reliance on VDP during original prosecution;
- Balaban’s disclosure of elements related to the ADC and the anti-aliasing filter as cited in Ground 3 and the Patent Office’s reliance on Balaban during original prosecution;
- Tsividis’ disclosure of the transconductance (gmC) filter function as cited in Ground 4; and
Greenberg’s disclosure of the FIR filter stored in memory as cited in Ground 5.

This Petition, supported by the Declaration of Dr. Hashemi, demonstrates that there is a reasonable likelihood that Petitioner will prevail with respect to at least one of the challenged claims and that each of the challenged claims is unpatentable for the reasons cited in this petition. (See 35 U.S.C. § 314(a.).)

IV. INVALIDITY OF THE ‘585 PATENT

A. Introduction

The ’585 patent, entitled “Broadband Receiver having a Multistandard Channel Filter,” claims priority to a provisional application filed on September 17, 2001, and was originally assigned to Xceive Corp. (Ex. 1101). Cresta Technology purchased certain of Xceive’s assets including the ’585 patent on October 10, 2011. (Ex. 1103, ITC Complaint, p.4.) In January, 2014, CrestaTech sued Petitioner and several of its customers for infringing two of the patents it acquired from Xceive. (Id.)

The ’585 patent admits that television receivers capable of receiving multiple different television standards such as NTSC and PAL were known in the art. An admitted “prior art” architecture of such a multistandard receiver is shown in Fig. 1 of the patent:
As shown above, that architecture included: a tuner for receiving an radio frequency (“RF”) input signal; a tuner for converting that RF signal to an intermediate frequency (“IF”) signal; a multichannel filter 18 comprised of a “bank of channel filters 18a to 18c,” each corresponding to a “specific format and standard”; and a demodulator 20 comprised of a plurality of individual demodulators, each “receiving filtered signals from a corresponding channel filter.” (Id. at 1:49–2:26). This “conventional multi-standard” television architecture could handle both analog and digital TV formats as well as different TV standards. (Id.)

The ’585 patent purports to solve the shortcomings of the prior art by processing the IF signal in the digital domain rather than in the analog domain. To accomplish this, the ’585 patent replaces the “bank of channel filters 18a to 18c” with a digital channel filter 58, as shown below:
This programmable channel filter converts the incoming analog IF signal to a digital representation (after performing anti-aliasing) using an analog-to-digital converter (“ADC”) 62 and then filters the digital signal in the digital domain using a digital signal processor (“DSP”) 64. The DSP implements one of several filter functions depending on the television format and standard of the incoming RF signal, as indicated by the “standard selection circuit 68.” The “coefficients of the filter functions” for each of those standard-specific filters “is stored in a look-up table in a memory 70.”

The ’585 patent is silent with respect improving TV broadcast reception quality. For example, the ’585 patent does not teach a system or method for increasing the video signal-to-noise ratio; the ’585 patent does not teach a system or method for improving RF front-end linearity; and the ’585 patent does not teach a system or method for improving the ability to block or exclude content on nearby
channels. (Ex. 1113, Hashemi’s Dec., ¶35.)

The ’585 patent is silent as to how one reasonably skilled in the art could actually make a tuner and a channel filter comprising an anti-aliasing filter, an analog-to-digital converter, a signal processor and a plurality of demodulators. (Id. at ¶36.)

The ’585 patent also is silent as to how “processing… in accordance with said format of said input RF signal” can actually be implemented and how that processing generates “digital output signals indicative of information encoded in said input RF signal” without ever decoding said information. (Id. at ¶37.)

For standards having an analog television format, the totality of what the ’585 patent says about actual “processing… in accordance with said format of said input RF signal” is as follows:

When the input RF signal is an analog television signal, DSP 64 applies a video filter function and a sound filter function to the digitized signals to separate the video signals from the audio signals. The video and sound filters can be implemented as FIR filters. An example of such filter function is shown in FIG. 5. (Ex. 1101; 5:23-28.) (Ex. 1113, Hashemi’s Dec., ¶38.)

The ‘585 patent only covers the architecture of a television receiver without disclosing circuit realizations for the analog to digital converter, the channel filters (FIR filters), or demodulators. (Id. at ¶37.)
B. Prosecution History of the ‘585 patent

The ’585 patent application was filed on September 6, 2002, and claims priority to Provisional Application No. 60/322,548, filed on September 17, 2001. In the first office action, all but three of the dependent claims were rejected in light of the prior art, which disclosed multi-mode receivers. Claims 1, 2, 5, 11, 13, 17–19\(^1\) and 23 were rejected under §102(e) “as being anticipated by Van De Plassche et al. [Ex. 1104, VDP].” (Ex. 1112, p. 55.) Claims 6, 12, 14–16, 20 and 21\(^2\) were likewise rejected under §103(a) “as being unpatentable over Van De Plassche et al.” (Ex. 1112, p. 56.) Claims 7, 8, 10 and 22\(^3\) were rejected as obvious “over Van De Plassche et al. in view of Balaban et al. [Ex. 1107, Balaban].” (Ex. 1112, p. 57.) Finally, claims 3, 4 and 9 “appear allowable over the prior art.” (Ex. 1112, p. 58.) In response to that office action, applicant submitted an amendment to incorporate the limitation of claim 3 as filed into the two independent claims 1 and 18 (now claim 17). Specifically, claim 1 was amended to add a “plurality of demodulators” as shown below:

---

\(^1\) Claims 2, 5, 11, 13, 17 and 19 (as filed) issued as Claims 2, 4, 10, 12, 16 and 18, respectively. (See Ex. 1110, p. 20.)

\(^2\) Claims 6, 12, 14–16, 20 and 21 (as filed) issued as Claims 5, 11, 13-15, 19 and 20, respectively. *Id.*

\(^3\) Claims 7, 8, 10 and 22 (as filed) issued as Claims 6, 7, 9 and 21, respectively. *Id.*
a plurality of demodulators, each coupled to receive output signals from said signal processor each of said demodulators for demodulating said digital output signals according to one of said formats of said input RF signal, each of said demodulators generating video and audio baseband signals corresponding to said format of said input RF signal

(Ex. 1112, p. 45.) The applicant made a similar amendment to claim 18 as filed (issued claim 17):

demodulating said processing digitized signals to generate baseband signals corresponding to said format of said input RF signal.

(Id. at 47.) In the accompanying remarks, the applicant explained that “claim 1 has been amendment [sic] to include the limitation in allowable claim 3…. Furthermore, in the present amendment, claim 18 has been amendment [sic] to include the limitation in claim 23 which is allowable for the same reasons claim 3 is allowable.” (Id. at 50.)

In the subsequent Office Action of December 6, 2005, the Examiner rejected claim 18 (issued claim 17) even in light of this amendment because it did not mirror that “plurality of demodulators” language in claim 3. Accordingly the Examiner rejected claim 18 (issued claim 17) and its dependent claims “as being anticipated by Van De Plassche et al.” (Ex. 1112, pp. 36, 37.) In response to this rejection, applicant expressly recited a “plurality of demodulators” in claim 18 as
filed (issued claim 17), as it had done in claim 1:

demodulating using a plurality of demodulators said processed
processing digitized signals to generate baseband signals
corresponding to said format of said input RF signal signals.

(Id. at 28.) In response to this amendment, the Examiner allowed all of the claims.

(See “Notice of Allowability,” id. at 18.)

C. Person of Ordinary Skill in the Art

A person of ordinary skill in the art at the time of the alleged invention of
the ’585 patent (“POSITA”) would have held at least a Masters of Science or
higher degree in electrical engineering, as well as about four years of substantial
experience designing or doing research in the area of wireless communication
receivers and integrated circuit realization of Radio Frequency, known as RF,
wireless communication receivers. (Ex. 1113, Hashemi’s Dec., ¶42.) Additional
education may compensate for less experience and vice-versa. The field to which
the ’585 patent is directed is the field of integrated circuits and Radio Frequency
communication receivers. Id. This is a very demanding field with little margin for
error that requires a high level of skill to practice. Id. The POSITA should have a
holistic knowledge of wireless communication systems; RF integrated circuits; and
analog, mixed-signal, and digital integrated circuits. Id.

V. CLAIM CONSTRUCTION
The claims in an *inter partes* review should be accorded the broadest reasonable construction, as commonly understood by those of ordinary skill in the art in view of the descriptions of the specification. (*See 37 C.F.R. § 42.100(b).* ) Petitioner contends that all of the terms in the challenged claims should be given their plain and ordinary meaning.

Because the standard for claim construction at the Patent Office is different from that used during a U.S. District Court litigation, the Petitioner expressly reserves the right to argue a different claim construction in litigation for any term of the ’585 patent, as appropriate in that proceeding.

**A. Summary of Claim Terms Construed**

The Petitioner proposes the following constructions:

<table>
<thead>
<tr>
<th>Term</th>
<th>Claims</th>
<th>Petitioner’s Construction</th>
</tr>
</thead>
<tbody>
<tr>
<td>“RF signal”</td>
<td>1, 10, 13, 15, 16, 17, 19 and 20</td>
<td>signal having a frequency between 10 kHz and 100 GHz</td>
</tr>
<tr>
<td>“format”</td>
<td>1-3, 10, 13, 25 and 17-20</td>
<td>distinct signal format, such as analog or digital</td>
</tr>
<tr>
<td>“video and audio baseband signals”</td>
<td>1</td>
<td>at least one signal without transmission modulation</td>
</tr>
<tr>
<td>“baseband signals”</td>
<td>17</td>
<td></td>
</tr>
<tr>
<td>“signal processor”</td>
<td>1, 3 and 10-13</td>
<td>digital module that processes</td>
</tr>
</tbody>
</table>
B. “RF signal”

The specification of the ’585 patent defines “RF” as an abbreviation for “radio frequency” (Ex. 1101, col. 1, l. 52), which The Authoritative Dictionary of IEEE Standards Terms identifies as a frequency roughly between 10 kHz and 100 GHz. (Ex. 1111, p 912.) The Petitioner construes “RF signal” as a “signal having a frequency between 10 kHz and 100 GHz.” The Petitioner’s construction is supported by Dr. Hashemi’s Declaration. (Ex. 1113, Hashemi’s Dec., ¶46.)

C. “format”

Independent claims 1 and 17 recite that the input RF signals encode information “in one of a plurality of formats” and require certain functionality that reference the “format” of the input RF signals. The specification draws a distinction between “formats” and “standards”: “Television signals are transmitted in analog or digital formats and in accordance with a variety of standards.” (Ex. 1101, 1:27–29 (emphasis added).) The specification further identifies “analog or digital TV” as examples of formats and “NTSC, PAL or SECAM” as examples of television standards. (Id. at 2:5–8.) The Petitioner construes “format” as “distinct signal format, such as analog or digital.” The Petitioner’s construction is supported by Dr. Hashemi’s Declaration. (Ex. 1113, Hashemi’s Dec., ¶¶47-48.)
D. “video and audio baseband signals” and “baseband signals”

The specification of the ’585 patent admits that it was known in the art that a demodulator for an analog television standard will output a video baseband signal and an audio baseband signal. (See, e.g. Ex. 1101, 2:17-26.) The specification of the ’585 patent also admits it was known in the art that a demodulator for a digital television standard will output one baseband signal – an MPEG data stream:

For analog television signal reception, the demodulator is a VIF/SIF module. The VIF/SIF module provides a video output called CVBS (Composite Video Baseband Signal) and audio outputs, such as MPX or A2. For digital television signal reception, the demodulator is a digital demodulator typically including a down-converter, an analog-to-digital converter and other supporting circuitry to perform the demodulation. The digital demodulator outputs data in a MPEG data stream.

(Ex. 1101, 2:17-26.) Since the ’585 patent specification clearly indicates that a demodulator for digital television formats will output one signal (i.e., a MPEG data stream), the terms “video and audio baseband signals [plural]” and “baseband signals [plural]” are broadly construed as “at least one signal without transmission modulation.” Furthermore, if “video and audio baseband signals” were construed to be, for example, “a video baseband signal and an audio baseband signal,” the “said format of said input RF signal” would be limited to analog television format.

*The Authoritative Dictionary of IEEE Standards Terms* defines “baseband
signaling” as “[t]he transmission of a signal at its original frequency, that is, not changed by modulation. Note: It can be an analog or a digital signal.” (Ex. 1111, p 87.)

The Petitioner therefore construes “video and audio baseband signals” and “baseband signals” as “at least one signal without transmission modulation.” The Petitioner’s construction is supported by Dr. Hashemi’s Declaration. (Ex. 1113, Hashemi’s Dec., ¶¶49-56.)

E. “signal processor”

The ’585 patent describes a “digital signal processor DSP 64 [that] processes the digital signals according to the television standard to which the input RF signal is encoded.” (Ex. 1101, 4:51–54.) “DSP 64 is a programmable and reconfigurable processor.” (Ex. 1101, 4:65.)

The signal processor in claims 1-16 is a digital signal processor (DSP). The signal processor in at least claim 11 comprises a programmable computing unit (e.g., an Arithmetic Logic Unit (ALU)) and is able to index memory. (Ex. 1113, Hashemi’s Dec., ¶¶57-62.)

Indexing memory to retrieve and apply one of a plurality of finite impulse response (FIR) filters indicates that the DSP implements a programmable filter. (Id.)

The specification supports a construction of “signal processor” that is
limited to digital signal processing. The Petitioner construes “signal processor” as “digital module that processes signals in the digital domain.” The Petitioner’s construction is supported by Dr. Hashemi’s Declaration. (*Id.*)

VI. DETAILED EXPLANATIONS OF THE CHALLENGES

Challenged claims 2-16 depend from independent challenged claim 1. Challenged claims 18-21 depend from independent challenged claim 17. A detailed explanation is provided below for each ground for each of the challenged claims, along with references to the supporting Declaration of Dr. Hashemi.

A. [GROUND 1] – VDP in View of Ishikawa Renders Claims 1, 2, 4, 5, 10 and 12-20 Unpatentable over under 35 U.S.C. § 103(a)

1. Motivation to Combine VDP and Ishikawa

Ishikawa and VDP both disclose multi-standard multi-format television receivers. (Ex. 1113, Hashemi’s Dec., ¶65.) Therefore, it would be natural for a POSTIA to take the teachings of these two patents to realize a multi-standard multi-format television receiver. (*Id.*) In fact, both of these patents cover receiver architectures where the IF signal is converted to a digital format using an ADC so that channel filtering and other processing can be performed in a digital signal processor. (*Id.*) It would be natural and expected that a POSTIA, interested in realizing a multi-standard television receiver with digital-IF, to combine the teachings of these patents. (*Id.*)

VDP was considered by the Examiner during prosecution of the ’585 patent.
Ishikawa overcomes the shortcomings identified by the Examiner during prosecution and was not considered by the Examiner.

VDP was relied upon by the Examiner to reject claims 1, 2, 4, 5 and 10-20 (as issued) of the ‘585 patent during original prosecution of the ‘585 patent. The Examiner identified all features of claims 1, 2, 4, 5 and 10-20 (as issued) in VDP, except for the “plurality of demodulators” limitation of claim 1 and “the “demodulating using a plurality of demodulators” limitation of claim 17. However, the Examiner did recognize that VDP anticipates the “demodulating said processed digitized signals to generate baseband signals corresponding to said format of said input RF signals” limitation. (See Exhibit 1112, File History of the ‘585 Patent, pp. 36-37 “VDP also includes demodulation of the processing digitized signal typical of a tuning receiver (SDEM in Fig. 5).”)

What is notable from this prosecution is the rejection that the Examiner did not make. (Ex. 1113, Hashemi’s Dec., ¶68.) The Examiner recognized that VDP anticipated the applicant’s original idea of a multi-standard broadband television receiver that processes and demodulates IF signals in the digital domain instead of the analog domain, but considered the notion of separate demodulators for each of those standards to be novel. (Id.) However, the inventors themselves admitted that the prior art used separate demodulators for different standards, as shown in Fig. 1 of the ‘585 patent (above). (Id.) Even if this was novel, which it was not, one
skilled in the art would have found this element to be obvious in view of the prior art. (Id.)

Despite allowance by the Examiner based on the plurality of demodulators feature of claims 1 and 17, this feature was well-known in the art prior at the time that the application for the ‘585 patent was filed. (Ex. 1113, Hashemi’s Dec., ¶¶69-71.) It was well-known that each of the plurality of demodulators would operate according to a format, such as an analog or a digital format. Id. Such knowledge is evidenced, for example, by the disclosure in Ishikawa. Id. Ishikawa’s receiver, comprising a plurality of demodulators, is suitable for analog and digital television formats. (See, e.g., id., 6:60-65 “Another object of the present invention is to provide a receiver which is capable of receiving signals by automatically discriminating between both kinds of modulated signals even when analog and digital modulated signals are mixed together in use in a ground wave TV broadcasting system and a cable transmission system.”)

A POSITA would be motivated to use Ishikawa’s design with a plurality of demodulators (shown below in orange annotation on Figure 14 of Ishikawa) to modify VDP’s design with a combined demodulator (shown below in orange annotation on Figure 5 of VDP). (Ex. 1113, Hashemi’s Dec., ¶¶69-71) Both Ishikawa and VDP digitally demodulate analog and digital formatted television signals. VDP uses a synchronous demodulator that combines the demodulation
functions. (See, e.g., Ex. 1104, VDP, 6:32-37). Ishikawa uses separate demodulators – one for analog formatted signals and one for digital formatted signals. (See, e.g., Ex. 1105, Ishikawa, 18: 3-5, describing a demodulator for a particular digital format standard, see also, e.g., id., 19:30-45 describing a demodulation for a particular analog format standard.) (Ex. 1113, Hashemi’s Dec., ¶¶69-71). A POSITA would be motivated to use Ishikawa’s modular system concept in order to add flexibility while implementing the demodulation functions. Id. A modular approach to hardware design enables the addition and removal of hardware elements while maintaining system integrity. Id.

Ishikawa discloses a communication receiver that is capable of receiving and demodulating multiple formats/standards. Id. In particular, it discloses a receiver that can operate for both analog and digital modulation formats, and a circuitry that can detect the modulation format and adjust the receiver parameters for proper operation. Id. The receiver includes a plurality of demodulators operating for analog and digital modulation formats. Id. The communication receiver disclosed in the Ishikawa patent includes a tuner that frequency down-converts the RF signals into an intermediate frequency, converts the IF signal from analog to digital format using an ADC, and perform modulation/format-specific channel filtering and demodulation. Id. The Ishikawa approach is general in that more demodulators can be easily added in parallel with the existing ones to support more modulation
formats and standards. *Id.* The aforementioned modular approach enables independent optimization or modification of each demodulator without necessarily affecting other demodulators. *Id.*

2. **Combining VDP and Ishikawa**

VDP states, “[t]here are numerous ways of physically spreading functions or functional elements over various units.” (Ex. 1104, VDP, 8:8-9.) VDP offers specific alternative arrangements with respect to figure 5. (Ex. 1113, Hashemi’s Dec., ¶¶72-74). For example, figure 5 of VDP shows digital filters after the demodulator. *Id.* As an alternative, VDP also teaches that the order the filtering and demodulation can be reversed, i.e., the digital filters can be placed before the demodulator:

With reference to FIG. 5, it should also be noted that any of the digital filters DF4-DF10 behind the synchronous demodulator SDEM may be replaced by a digital filter in front of the synchronous demodulator SDEM. If all the digital filters DF4-DF10 were replaced in this manner, the filter arrangement FIL would not comprise a synchronous demodulator.

(Ex. 1104, VDP, 9:3-9.) According to VDP’s alternative arrangement of figure 5, the demodulator is placed after the digital filters, as shown below:
Also, for clarity, two filters, two sample rate reduction circuits and the AFRC have been consolidated into a block labeled AFRC in figure 5. In figure 5 as annotated above, the AFRC block performs digital processing functions within VDP’s signal processor. *(Id.)* The processing represented by the AFRC block is shown below:

(Ex. 1104, VDP, Fig. 5 annotation added.) (Ex. 1113, Hashemi’s Dec., ¶¶ 71-74.)

Figure 14 in Ishikawa (below) illustrates a receiver structure comprising an
analog modulated signal demodulator and a digital modulated signal demodulator.

(See, e.g., Ex. 1105, Ishikawa, 18: 3-5, describing a demodulator for a particular digital format standard, see also, e.g., id., 19:30-45 describing a demodulation for a particular analog format standard).

Figure 5 of VDP and figure 14 of Ishikawa will be used to illustrate limitation in the challenged claims.

Claims 1 and 17 are the only impendent claims. Claim 1 recites a receiver, while claim 17 recites “[a] method for receiving input RF signal.” According to the Applicant, claims 1 and 17 were drafted to have the same scope. (See Exhibit

(Ex. 1105, Ishikawa, Fig. 14, annotation added.) (Ex. 1113, Hashemi’s Dec., ¶75.)
Under the broadest reasonable interpretation, Petitioner submits that the preambles of claims 1 and 17 are not limiting. However, even if the preambles are limiting, both VDP and Ishikawa teach a receiver and a method for receiving input RF signals. (Ex. 1113, Hashemi’s Dec., ¶77.)

VDP’s tuner is shown above in red annotation on Figure 5 of VDP. VDP describes a tuner for receiving Srf (i.e., “input RF signals”) and converting said input RF signals to Sif (i.e., “intermediate signals having an intermediate frequency.”) The information in the input RF signals in both VDP and Ishikawa is encoded in one of a plurality of formats, including analog and digital television formats. (Ex. 1113, Hashemi’s Dec., ¶78.)

VDP’s channel filter comprising an anti-aliasing filter (AAF); an analog-to-digital converter (ADC); and a signal processor. VDP’s anti-aliasing filter is shown above in green annotation on Figure 5 of VDP, and the AAF symbol is reproduced below. (Ex. 1113, Hashemi’s Dec., ¶79.)

(Ex. 1104, VDP, Fig. 5) The three-wave symbol with the higher and lower waves
crossed indicates a bandpass filter, which comprises a center frequency by definition. (Ex. 1113, Hashemi’s Dec., ¶80.)

VDP’s analog-to-digital converter is shown above in blue annotation on Figure 5 of VDP. Ishikawa’s analog-to-digital converter is shown above in blue annotation on Figure 14 of Ishikawa. (Ex. 1113, Hashemi’s Dec., ¶¶73-85.) VDP’s signal processor is shown above in pink annotation on Figure 5 of VDP. (Id.) Ishikawa’s signal processor is shown above in pink annotation on Figure 14 of Ishikawa. (Id.) The signal processors in both VDP and Ishikawa process said digitized signals in accordance with said format of said input RF signals and generate digital output signals indicative of information encoded in said input RF signals. (Id.)

VDP’s combined demodulator, SDEM, in Figure 5 above performs all functionality required for analog television demodulation and digital television demodulation. (Id.) Therefore, Ishikawa’s plurality of demodulators in Figure 14 of Ishikawa above is not cited to replace the functionality VDP’s combined demodulator. Ishikawa discloses an alternative structure for the functionality that already exists in VDP. (Id.)

As shown in orange annotation on Figure 14 of Ishikawa, above, each demodulator in Ishikawa’s plurality of demodulators is coupled to receive digital output signals and demodulate said digital output signals according to one of said
formats of said input RF signals as required in claim 1. (*Id.*)

Ishikawa teaches that is was known that the structures for analog television
demodulation and digital television demodulation could be completely separated in
a multi-standard television receiver, as evidenced in figure 14 where the
demodulator structure for digital format comprises at least Digital Data Detector
521 and the demodulator structure for analog format comprises at least Frequency
Detector 531, De-Emphasis Circuit 532, and Clamper 533. (*Id.*) Moreover,
Ishikawa illustrates that the input to each of the separate demodulator structures
comes from a common digital module (comprising Complex Multipliers 513 and
517; Digital LPF’s 514 and 515; and Detector 519) that processes signals in the
digital domain. (*Id.*)

Furthermore, the combination of VDP and Ishikawa does not change the
principle of operation of VDP or render VDP inoperable for its intended purpose.
(*Id.*) Ishikawa merely teaches an alternative structural arrangement to perform the
same function, i.e., each of Ishikawa’s plurality of demodulators are
“demodulating said digital output signals according to one of said formats of said
input RF signal.” (*Id.*)

With respect to claim 12, VDP clearly shows and states that the single real
signal at IF (referred to as a scalar signal) is filtered with “two different finite
impulse responses Ax(z) and Ay(z) provided by the digital filter DF1.” (*See Ex.
In Fig. 5 of VDP, it is clearly shown that the single output signal from the analog-to-digital converter (ADC) enters \( Ax(z) \) and \( Ay(z) \) in parallel to produce XIF and YIF. \( Id. \) DF1 is a filter whose output is a weighted sum of the current and a finite number of past inputs. \( Id. \) \( Ax(z) \) the real part of the weighted sum operation. \( Id. \) \( Ay(z) \) the imaginary part of the weighted sum operation. \( Id. \) XIF is the real part of the weighted sum output. \( Id. \) YIF is the imaginary part of the weighted sum output. (\( Id.; \) Ex. 1113, Hashemi’s Dec., \( ¶\¶ \)98-100.)

Claims 13-15 and 19-20 simply require that the specific digital signal processing performed on a digital representation of the information waveform can be in response to a select signal that indicates the format of the original RF waveform, that select signal can be a user input for example. (\( Id. \) at \( ¶\¶ \)101-102) In a multi-standard or multi-format communication receiver, including TV receivers, it is obvious that specific settings for each of the building blocks and processes, including digital signal processing, can be through select signals that are indicative to a specific standard or format. (\( Id. \)) In fact, using select signals, corresponding to specific standards or formats, to select specific building blocks, functions, or processes is the most obvious and natural approach towards realization of a multi-standard or multi-format communication receiver, including a television receiver. (\( Id. \)) Furthermore, these claim was specifically taught in the very context of TV
receivers in Ishikawa. In summary, Claims 13-15 and 19-20 of ‘585 do not teach anything new to a POSITA at the time of ‘585 filing. (Id.)

<table>
<thead>
<tr>
<th>‘585 Patent – Claim 1</th>
<th>VDP (Ex. 1104) and Ishikawa (Ex. 1105)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. A receiver comprising:</td>
<td>See, e.g., Ex. 1104, VDP, 1:5 (“invention relates to the reception of signals.”) see also Ex. 1113, Hashemi’s Dec., ¶86-92.</td>
</tr>
</tbody>
</table>
| a tuner for receiving input RF signals and for converting said input RF signals to intermediate signals having an intermediate frequency (IF), | See, e.g., Ex. 1104, VDP, 3:2-3 (“A tuner TUN converts a reception signal Srf to an intermediate-frequency signal Sif.”)  

See also Ex. 1104, VDP, Fig. 5 (showing a tuner TUN receiving Srf and outputting Sif); (Ex. 1113, Hashemi’s Dec., ¶87. |
| said input RF signals encoding information in one of a plurality of formats; | See, e.g., Ex. 1104, VDP, 6:1-12 (“The invention relates to the reception of signals which are transmitted in accordance with different standards. For example, television (TV) signals are transmitted in accordance with different standards depending on the country or region and/or depending on the type of transmission which may be analog or digital, via cable, satellite or a terrestrial path.”).  

See, e.g., Ex. 1105, Ishikawa, 6:60-65 (“Another object of the present invention is to provide a receiver which is capable of receiving signals by automatically discriminating between both kinds of modulated signals even when analog and digital modulated signals are mixed together in use in a ground wave TV broadcasting system and a cable transmission system.”).  

See also Ex. 1113, Hashemi’s Dec., ¶86-87. |
<p>| a channel filter for receiving the intermediate signals, said channel filter comprising: | See, e.g., Ex. 1104, VDP, 5:4-12 (“In the FIG. 5 receiver, the following additional elements are coupled between the tuner TUN and the controllable frequency converter AFRC: an anti-aliasing filter AAF, an analog-to-digital converter ADC which includes the |</p>
<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sampling circuit S&amp;H</td>
<td>a digital filter DF1 and a sample-rate decreaser SRD1. The filter arrangement FIL includes various digital filters DF2—DF10, two sample rate decreasers SRD2, SRD3, and a synchronous demodulator SDEM.</td>
</tr>
</tbody>
</table>

See also, e.g., VDP, Fig. 5 (showing AAF, ADC, and digital filters DF1-DF10).

see also Ex. 1113, Hashemi’s Dec., ¶88.

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Anti-aliasing filter</td>
<td>for filtering said intermediate signals;</td>
</tr>
</tbody>
</table>

See, e.g., Ex. 1104, VDP, 5:4-12 (“In the FIG. 5 receiver…: an anti-aliasing filter AAF”).

See also, e.g., VDP, Fig. 5 (showing an anti-aliasing filter).

see also Ex. 1113, Hashemi’s Dec., ¶88.

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog-to-digital converter</td>
<td>for sampling said filtered intermediate signals and generating a digital representation thereof;</td>
</tr>
</tbody>
</table>

See, e.g., Ex. 1104, VDP, 5:4-12 (“In the FIG. 5 receiver… an analog-to-digital converter ADC”).

See also, e.g., Ex. 1104, VDP, Fig. 5 (showing ADC).

see also, e.g., Ishikawa, Fig. 14 (showing A/D 511 and 512).

see also Ex. 1113, Hashemi’s Dec., ¶88.

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Signal processor</td>
<td>for processing said digital representation of said intermediate signals</td>
</tr>
</tbody>
</table>

Ex. 1104, VDP, 8:43-51 (“It should also be noted that various functions or functional elements may be implemented by means of a suitably programmed computer, either individually or in combination. For example, with reference to FIG. 5, the filter arrangement FIL may be implemented in the form of a signal processor. The signal processor may also comprise other functional elements such as the sound processor SPRC, the video processor VPRC and/or the symbol processor XPRC.”)

See, e.g., Ex. 1104, VDP, 5:4-12 (“In the FIG. 5 receiver... a digital filter DF1... various digital filters...”)
<table>
<thead>
<tr>
<th>Cell 1</th>
<th>in accordance with said format of said input RF signal, said signal processor generating digital output signals indicative of information encoded in said input RF signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cell 2</td>
<td>See also, e.g., Ex. 1104, VDP, 8:38-43 (“the assembly of digital filters DF4-DF10 may be replaced by a single adjustable filter which can provide various frequency responses for suitably processing any content which may be comprised in the vectorial baseband signal Svbb.”);</td>
</tr>
<tr>
<td></td>
<td>See also, e.g., Ex. 1105, Ishikawa, 17:18-25 (“The digital LPFs 514 and 515 operate as filters for removing high frequency components from their input signals if the input signals include the FM signal. While if the input signals include the QPSK modulated signal, they operate as filters for providing transfer characteristics required for preventing an inter-symbol interference in the digital data transmission.”);</td>
</tr>
<tr>
<td></td>
<td>see also Ex. 1113, Hashemi’s Dec., ¶89.</td>
</tr>
</tbody>
</table>
a plurality of demodulators, each coupled to receive output signals from said signal processor: each of said demodulators for demodulating said digital output signals according to one of said formats of said input RF signal, each of said demodulators

Ex. 1105, Ishikawa, 18: 3-5 (“If the IF signal includes the QPSK modulated signal, the digital data detector 521 demodulates the QPSK data.”)

Ex. 1105, Ishikawa, 19:30-45 (“The output (frequency component) of the frequency detector 531 is supplied to the de-emphasis circuit 532. The de-emphasis circuit 532 includes a circuit that has a characteristics contrary to a pre-emphasis performed at the transmitter side and by attenuating high frequency components, restores the received signal to the signal having an original flat frequency characteristics. The output of the de-emphasis circuit 532 is supplied to a clamer 533 and a sync separator 537. The sync separator 537 separates sync signal from input signal and based on the sync signal, provides clamp pulse to the clamer 533. Thus, DC regeneration is carried out in the clamer 533 and the DC regenerated FM demodulated signal is converted to analog signal in a D/A converter 534 and is led to an FM demodulated signal output terminal 536.”)

*see also* Ex. 1113, Hashemi’s Dec., ¶¶90-91.

generating video and audio baseband signals corresponding to said format of said input RF signal.

See, e.g., Ex. 1104, VDP, 8:38-43 (“The synchronous demodulator SDEM effectively shifts a desired main carrier, Which is comprised in the input signal Sin, to Zero (0) frequency. As a result, a vectorial baseband signal Svbb is obtained. It is composed of two components Xbb and Ybb corresponding to an in-phase and a quadrature modulation-component of the main carrier.”); *see also* Ex. 1113, Hashemi’s Dec., ¶¶90-91.

<table>
<thead>
<tr>
<th>‘585 Patent – Claim 2</th>
<th>VDP (Ex. 1104) and Ishikawa (Ex. 1105)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2. The receiver of claim 1, wherein said plurality of formats comprise an analog television format and a digital television format.</td>
<td>See above discussion of ‘585 patent, claim 1.</td>
</tr>
<tr>
<td></td>
<td>See, e.g., Ex. 1104, VDP, 1:9-10; (“the type of transmission which may be analog or digital”); <em>see also</em>, e.g., Ex. 1105, Ishikawa, 18: 3-5 and</td>
</tr>
</tbody>
</table>
‘585 Patent – Claim 4

<table>
<thead>
<tr>
<th>VDP (Ex. 1104) and Ishikawa (Ex. 1105)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4. The receiver of claim 1, wherein said intermediate frequency comprises</td>
</tr>
<tr>
<td><em>See</em> above discussion of ‘585 patent, claim 1.</td>
</tr>
<tr>
<td>a frequency value specified by one or more television standards</td>
</tr>
<tr>
<td><em>See, e.g.,</em> Ex. 1104, VDP, 5:18-20 (“the tuner TUN provides the intermediate-frequency signal Sif at one of the typically used intermediate frequencies listed below.”); and Ex. 1104, VDP, 5:22-29:</td>
</tr>
<tr>
<td>analog terrestrial TV transmissions</td>
</tr>
<tr>
<td>Europe</td>
</tr>
<tr>
<td>America</td>
</tr>
<tr>
<td>Japan</td>
</tr>
<tr>
<td><em>see also</em> Ex. 1113, Hashemi’s Dec., ¶94.</td>
</tr>
</tbody>
</table>

‘585 Patent – Claim 5

<table>
<thead>
<tr>
<th>VDP (Ex. 1104) and Ishikawa (Ex. 1105)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5. The receiver of claim 1, wherein said intermediate frequency comprises</td>
</tr>
<tr>
<td><em>See</em> above discussion of ‘585 patent, claim 1.</td>
</tr>
<tr>
<td>a frequency value other than those specified by one or more television standards.</td>
</tr>
<tr>
<td><em>See, e.g.,</em> Ex. 1104, VDP, 5:18-20 (“For any one of a large number of different intermediate frequencies, the adjustable frequency converter can be adjusted in such a way that the filter arrangement receives the input signal in a frequency range which is suitably located with respect to the frequency responses it provides.”);</td>
</tr>
<tr>
<td><em>see also</em> Ex. 1104, VDP 2:4-2:16 and 9:10-9:21;</td>
</tr>
<tr>
<td><em>see also</em> Ex. 1113, Hashemi’s Dec., ¶95.</td>
</tr>
</tbody>
</table>

‘585 Patent – Claim 10

<table>
<thead>
<tr>
<th>VDP (Ex. 1104) and Ishikawa (Ex. 1104)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10. The receiver of claim 1,</td>
</tr>
<tr>
<td><em>See</em> above discussion of ’585 patent, claim 1.</td>
</tr>
<tr>
<td>*585 Patent – Claim 12</td>
</tr>
<tr>
<td>------------------------</td>
</tr>
<tr>
<td>12. The receiver of claim 10, wherein said signal processor comprises a first computing unit and a second computing unit, said first computing unit processing a real part of said finite impulse response filter operation while said second computing unit processing an imaginary part of said finite impulse response filter operation.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>*585 Patent – Claim 13</th>
<th>VDP (Ex. 1104), Ishikawa (Ex. 1105)</th>
</tr>
</thead>
<tbody>
<tr>
<td>13. The receiver of claim 10, wherein said channel filter further comprises a standard selection circuit coupled to said signal processor, said standard</td>
<td>See above discussion of ’585 patent, claim 10. See, e.g., Ex. 1105, Ishikawa, abstract (“a controller for controlling the demodulator to be able to discriminate between the analog modulated</td>
</tr>
</tbody>
</table>
selection circuit generating a select signal indicative of a format of said input RF signal and said signal processor selecting a finite impulse response filter in response to said select signal.

signals and the digital modulated signals, based on a demodulated signal output from the digital section of the demodulator and to be switched into a demodulation mode suited for modulation system of the selected channel of the high frequency signals.”;

See, e.g., Ex. 1105, Ishikawa 8:64-9:12; FIG. 7(B) (“a diagram showing a definite example of the digital modulation discriminator”); FIG. 8(A) (“a diagram showing another example of the transmission signal format according to the present invention”); FIG. 8(B) (“a diagram showing an example of the digital modulation discriminator 300 in FIG. 6”); FIG. 9(A) (“a diagram showing an example of the spectrum of the transmission signal according to the present invention”); FIG. 9(B) (“a diagram showing another example of the digital modulation discriminator 300 in FIG. 6”); FIG. 10(A) (“a diagram showing vector phases of the transmission signal modulation system according to the present invention”); and FIG. 10(B) (“a diagram showing still another example of the digital modulation discriminator 300 in FIG. 6”).

See, e.g., Ex. 1105, Ishikawa, 17:18-25 (“The digital LPFs 514 and 515 operate as filters for removing high frequency components from their input signals if the input signals include the FM signal. While if the input signals include the QPSK modulated signal, they operate as filters for providing transfer characteristics required for preventing an inter-symbol interference in the digital data transmission.”);

*see also* Ex. 1113, Hashemi’s Dec., ¶¶101-102.

<table>
<thead>
<tr>
<th>‘585 Patent – Claim 14</th>
<th>VDP (Ex. 1104) and Ishikawa (Ex. 1105)</th>
</tr>
</thead>
<tbody>
<tr>
<td>14. The receiver of claim 13, wherein said standard</td>
<td><em>See</em> above discussion of ’585 patent, claim 13.</td>
</tr>
</tbody>
</table>
| **selection circuit generates said select signal** | **See, e.g., Ex. 1105, Ishikawa, 3:51-55 ("In the arrangement as described above, however, each of the analog and digital demodulators is independent and thus users must know in advance a modulation satellite system by which a signal is transmitted or broadcasted and then select an adequate demodulator.")**

*see also* Ex. 1113, Hashemi’s Dec., ¶¶101-102. |
|---|---|

<table>
<thead>
<tr>
<th><strong>‘585 Patent – Claim 15</strong></th>
<th><strong>VDP (Ex. 1104) and Ishikawa (Ex. 1105)</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>15. The receiver of claim 13, wherein said standard selection circuit generates said select signal</td>
<td><strong>See above discussion of ‘585 patent, claim 13.</strong></td>
</tr>
</tbody>
</table>

*See, e.g., Ex. 1105, Ishikawa, 12:3-15 ("FIG. 9(A-b) shows the spectrum of the VSB-AM signal of an NTSC composite signal. The video carrier frequency is at a position lower than the center by 1.75 MHz. Therefore, frequencies of the QAM and the VSB-AM modulated carrier frequencies differ from each other by the 1.75 MHz. Accordingly, if the frequency error is large when inspecting the frequency error of the detected output, in other words, if the loop filter output is larger than a prescribed amount it may be better to determine that the modulated signal includes the VSB-AM signal, or if the loop filter output is smaller than the prescribed amount it may be determined to include the QAM signal."); see also* Ex. 1113, Hashemi’s Dec., ¶¶101-102. |

<table>
<thead>
<tr>
<th><strong>‘585 Patent – Claim 16</strong></th>
<th><strong>VDP (Ex. 1104) and Ishikawa (Ex. 1105)</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>16. The receiver of claim 1, wherein said input RF signals comprise RF signals received from</td>
<td><strong>See above discussion of ‘585 patent, claim 1.</strong></td>
</tr>
</tbody>
</table>

*See, e.g., Ex. 1104, VDP, 1:8-12 ("television (TV)

---

**41**
one of terrestrial broadcast, from satellite broadcast, and from cable transmission.  

<table>
<thead>
<tr>
<th>'585 Patent – Claim 17</th>
<th>VDP (Ex. 1104) and Ishikawa (Ex. 1105)</th>
</tr>
</thead>
<tbody>
<tr>
<td>17. A method for receiving input RF signal comprising:</td>
<td>See, e.g., Ex. 1104, VDP, 1:5 (“invention relates to the reception of signals.”); and 3:2 (“a reception signal Srf.”); see also Ex. 1113, Hashemi’s Dec., ¶¶69.</td>
</tr>
<tr>
<td>receiving said input RF signals encoding information in one of a plurality of formats;</td>
<td>See the “said input RF signals encoding information in one of a plurality of formats” limitation of claim 1, above.</td>
</tr>
<tr>
<td>converting said input RF signals to intermediate signals having an intermediate frequency;</td>
<td>See the “a tuner for receiving input RF signals and for converting said input RF signals to intermediate signals having an intermediate frequency (IF)” limitation of claim 1, above.</td>
</tr>
<tr>
<td>applying a first filter function to said intermediate signals, said first filter function being an anti-aliasing filter and having a center frequency;</td>
<td>See the “an anti-aliasing filter for filtering said intermediate signals” limitation of claim 1, above.</td>
</tr>
<tr>
<td>digitizing said filtered intermediate signals at a sampling frequency;</td>
<td>See the “an analog-to-digital converter for sampling said filtered intermediate signals and generating a digital representation thereof” limitation of claim 1, above.</td>
</tr>
</tbody>
</table>

signals are transmitted in accordance with different standards depending on the country or region and/or depending on the type of transmission which may be analog or digital, via cable, satellite or a terrestrial path.”);  

See, e.g., Ex. 1105, Ishikawa, 6:60-65 (“Another object of the present invention is to provide a receiver which is capable of receiving signals by automatically discriminating between both kinds of modulated signals even when analog and digital modulated signals are mixed together in use in a ground wave TV broadcasting system and a cable transmission system.”);  

see also Ex. 1113, Hashemi’s Dec., ¶¶69.
<table>
<thead>
<tr>
<th><strong>processing</strong></th>
<th>See the “a signal processor for processing” limitation of claim 1, above.</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>said digitized signals</strong></td>
<td>See the “said digital representation of said intermediate signals” limitation of claim 1, above.</td>
</tr>
<tr>
<td>in accordance with said format of said input RF signals and generating digital output signals indicative of information encoded in said input RF signals</td>
<td>See the “in accordance with said format of said input RF signal, said signal processor generating digital output signals indicative of information encoded in said input RF signal” limitation of claim 1, above.</td>
</tr>
<tr>
<td><strong>demodulating using a plurality of demodulators</strong></td>
<td>See the “a plurality of demodulators, each coupled to receive output signals from said signal processor, each of said demodulators for demodulating said digital output signals according to one of said formats of said input RF signal,” limitation of claim 1, above.</td>
</tr>
<tr>
<td><strong>[demodulating] said processed digitized signals to generate baseband signals corresponding to said format of said input RF signals</strong></td>
<td>See the “each of said demodulators generating video and audio baseband signals corresponding to said format of said input RF signal” limitation of claim 1, above.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>‘585 Patent – Claim 18</strong></th>
<th>VDP (Ex. 1104) and Ishikawa (Ex. 1105)</th>
</tr>
</thead>
<tbody>
<tr>
<td>18. The method of claim 17, wherein said plurality of formats comprise an analog television format and a digital television format.</td>
<td>See above discussion of ‘585 patent, claim 17. See the “analog television format and a digital television format” limitation of claim 2, above. See also Ex. 1113, Hashemi’s Dec., ¶107.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>‘585 Patent – Claim 19</strong></th>
<th>VDP (Ex. 1104) and Ishikawa (Ex. 1105)</th>
</tr>
</thead>
<tbody>
<tr>
<td>19. The method of claim 17, wherein said processing said digital signals is</td>
<td>See above discussion of ’585 patent, claim 17.</td>
</tr>
</tbody>
</table>
performed in response to a select signal indicative of said format of said input RF signal. 

See above discussion of ’585 patent, claim 13; see also Ex. 1113, Hashemi’s Dec., ¶108.

<table>
<thead>
<tr>
<th>‘585 Patent – Claim 20</th>
<th>VDP (Ex. 1104) and Ishikawa (Ex. 1105)</th>
</tr>
</thead>
<tbody>
<tr>
<td>20. The method of claim 19, further comprising: generating said select signal</td>
<td>See above discussion of ’585 patent, claim 19.</td>
</tr>
<tr>
<td>by detecting carrier signals in said input RF signal identifying said format of said input RF signal</td>
<td>See above discussion of ’585 patent, claim 15; see also Ex. 1113, Hashemi’s Dec., ¶109.</td>
</tr>
</tbody>
</table>


1. Motivation to Combine VDP, Ishikawa and Malkemes

Ishikawa, Malkemes and VDP all disclose multi-standard multi-format television receivers. (Ex. 1113, Hashemi’s Dec., ¶¶110-112.) Therefore, it would be natural for a POSTIA to take the teachings of these patents to realize a multi-standard multi-format television receiver. (Id.) In fact, all these patents cover receiver architectures where the IF signal is converted to a digital format using an ADC so that channel filtering and other processing can be performed in a digital signal processor. (Id.) It would be natural and expected that a POSTIA, interested in realizing a multi-standard television receiver with digital-IF, to combine the teachings of these patents. (Id.)

Malkemes teaches a multi-standard television receiver that processes digital
IF signals. (Id.) Therefore, a POSITA would be motivated to use concepts from Malkemes with VDP in view of Ishikawa, which also teaches a multi-standard television receiver that processes digital IF signals. (Id.) The motivation to combine VDP and Ishikawa is described in section VI.A above. A POSITA would have incorporated Malkemes’ digital-to-analog converter according the input requirements of a subsequent demodulator. (Id.)

Malkemes discloses a communication receiver, specifically a television receiver that is capable of receiving and demodulating multiple standards. (Id.) Specifically, the television receiver down-converts the RF signals to an intermediate frequency, converts the IF signal to a digital format using an ADC, and provides standard-specific channel filtering in the digital domain. The patent covers several variations. (Id.) For instance, it demonstrates that the digitally processed and filtered IF signal can be converted to analog format using a DAC for interfacing with the following analog blocks such as analog demodulators. (Id.) In another variation, the patent demonstrates that demodulation and decoding can occur in the digital domain after digital channel filtering, and that the demodulated and decoded signals can be connected to display, speakers, etc. (Id.)

2. Combining VDP, Ishikawa and Malkemes

Malkemes signal processor comprises digital filters 144 and 154. (Ex. 1113, Hashemi’s Dec., ¶¶113-115.) Malkemes NTSC/PAL Decoder 200 comprises a
demodulator. (See, e.g., Ex. 1106, Malkemes, 20:31-21:1 “Circuits 210, 220, and 240 may employ known standard circuits and techniques to detect, demodulate and decode the NTSC/PAL signals.”)

As illustrated below, Malkemes comprises a digital-to-analog converter 160 coupled between a signal processor and at least one demodulator. (See, e.g., Ex. 1106, Malkemes, 19:10-14 “Digital-to-analog converter (DAC) and reconstruction filter apparatus 160 of receiver integrated circuit 100' processes the complex in-phase and quadrature digital signals from digital filters 144, 154 to produce two streams of digital data words, each preferably of 10-12 bits, that represent the information-bearing signals at an intermediate frequency.”). (Ex. 1113, Hashemi’s Dec., ¶¶113-115):
The digital-to-analog converter 160 also converts the digital output signals to an analog format. (Ex. 1113, Hashemi’s Dec., ¶¶115.)

<table>
<thead>
<tr>
<th>‘585 Patent – Claim 3</th>
<th>VDP (Ex. 1104), Ishikawa (Ex. 1105) and Malkemes (Ex. 1106)</th>
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</thead>
<tbody>
<tr>
<td>3. The receiver of claim 1, further comprising:</td>
<td>See above discussion of ’585 patent, claim 1.</td>
</tr>
<tr>
<td>a digital-to-analog converter coupled between said signal processor and a first one of said plurality of demodulators, said digital-to-analog converter converting said digital output signals to an analog format.</td>
<td>See, e.g., Ex. 1106, Malkemes, 9:1-10 (“the digital signals are reconverted in to an analog output signal at the IF frequency by the DAC thereof”); see also Ex. 1113, Hashemi’s Dec., ¶¶113-115</td>
</tr>
</tbody>
</table>

C. [GROUND 3] – VDP in view of Ishikawa and Balaban Renders Claims 6, 7, 9 and 21 Unpatentable under 35 U.S.C. § 103(a)

1. Motivation to Combine VDP, Ishikawa and Balaban

Ishikawa, VDP, and Balaban all disclose multi-standard multi-format television receivers. (Ex. 1113, Hashemi’s Dec., ¶¶117-120.) Therefore, it would be natural for a POSTIA to take the teachings of these patents to realize a multi-standard multi-format television receiver. (Id.) In fact, all these patents cover receiver architectures where the IF signal is converted to a digital format using an ADC so that channel filtering and other processing can be performed in a digital signal processor. (Id.) It would be natural and expected that a POSTIA, interested
in realizing a multi-standard television receiver with digital-IF, to combine the teachings of these patents. \((Id.)\)

Balaban teaches a multi-standard television receiver that processes digital IF signals. \((Id.)\) Therefore, a POSITA would be motivated to use concepts from Balaban with VDP in view of Ishikawa, which also teaches a multi-standard television receiver that processes digital IF signals. \((Id.)\) The motivation to combine VDP and Ishikawa is described in section VI.A above.

It would have been obvious to incorporate the anti-aliasing filter and analog-to-digital converter of Balaban with VDP and Ishikawa to avoid the introduction of aliasing signals into the sampled signal components that would not be removed by subsequent processing of the digital signal by NTSC and ATSC processing sections. \((Id.)\)

A POSITA would have incorporated the 10 bit analog-to-digital converter of Balaban with VDP and Ishikawa to increase sample resolution, which may improve reception quality. \((Id.)\)

2. **Combining VDP, Ishikawa and Balaban**

Balaban teaches that the center frequency of said anti-aliasing filter and a sampling frequency of said analog-to-digital converter are functions of said intermediate frequency. \((See, \textit{e.g.}, \text{Ex. 1107, Balaban, 4:61-5:3} “The sampling frequency } f_s \text{ is selected so that the frequency translated IF center frequency is} \)
greater than one half the desired signal bandwidth and so that the absolute value of
the frequency translated IF center frequency is greater than the desired signal
bandwidth. This avoids the introduction of aliasing signals into the sampled signal
components that would not be removed by subsequent processing of the digital
signal by NTSC and ATSC processing sections 140, 150.”; Ex. 1113, Hashemi’s
Dec., ¶¶121-123.)

Balaban teaches a tuning control circuit 160 for adjusting said center
frequency and said sampling frequency to frequency values derived from said
intermediate frequency. (Id.)

(Ex. 1107, Balaban, Fig. 2, annotation added.)

With respect to claim 9, Balaban teaches a 10-bit analog-to-digital converter.
(See, e.g., Ex. 1107, Balaban, 4:42-43 “A/D converter 130 is typically a 10-bit A/D
6. The receiver of claim 1, wherein

<table>
<thead>
<tr>
<th>'585 Patent – Claim 6</th>
<th>VDP (Ex. 1104), Ishikawa (Ex. 1105) and Balaban (Ex. 1107)</th>
</tr>
</thead>
<tbody>
<tr>
<td>a center frequency of said anti-aliasing filter and a sampling frequency of said analog-to-digital converter are functions of said intermediate frequency</td>
<td>See, e.g., Ex. 1107, Balaban, 4:61-5:3 (“The sampling frequency fs is selected so that the frequency translated IF center frequency is greater than one half the desired signal bandwidth and so that the absolute value of the frequency translated IF center frequency is greater than the desired signal bandwidth. This avoids the introduction of aliasing signals into the sampled signal components that would not be removed by subsequent processing of the digital signal by NTSC and ATSC processing sections 140, 150.”); see also Ex. 1113, Hashemi’s Dec., ¶¶121, 122, and 124.</td>
</tr>
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7. The receiver of claim 6, wherein

<table>
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<tr>
<th>'585 Patent – Claim 7</th>
<th>VDP (Ex. 1104), Ishikawa (Ex. 1105) and Balaban (Ex. 1107)</th>
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</thead>
<tbody>
<tr>
<td>said channel filter further comprises a tuning control circuit for adjusting said center frequency and said sampling frequency to frequency values derived from said intermediate frequency</td>
<td>See also, e.g., Ex. 1107, 6:46-51 (“Balaban Control circuit 160 may also include a second switching function within switch 162 where it is desired that A/D converter 130 operate at different sampling frequencies as a function of the format of the received signals. A first sampling frequency signal f_{sa} is provided through switch 162 as sampling signal f_{s} when signals in the analog signal format are received and a second sampling frequency signal f_{sd} is provided as sampling signal f_{s} when signals in the digital signal format are received.”); See also, e.g., Ex. 1107, Balaban, Fig. 2, Control Circuit 160 (showing the sampling frequency going</td>
</tr>
<tr>
<td>‘585 Patent – Claim 9</td>
<td>VDP (Ex. 1104), Ishikawa (Ex. 1105) and Balaban (Ex. 1107)</td>
</tr>
<tr>
<td>-----------------------</td>
<td>-------------------------------------------------------------</td>
</tr>
<tr>
<td>9. The receiver of claim 1, wherein</td>
<td>See above discussion of ‘585 patent, claim 1.</td>
</tr>
<tr>
<td>said analog-to-digital converter is a 10-bit converter</td>
<td>See, e.g., Ex. 1107, Balaban, 4:42-43 (“A/D converter 130 is typically a 10-bit A/D converter.”); see also Ex. 1113, Hashemi’s Dec., ¶¶123 and 126.</td>
</tr>
</tbody>
</table>

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<thead>
<tr>
<th>‘585 Patent – Claim 21</th>
<th>VDP (Ex. 1104), Ishikawa (Ex. 1105) and Balaban (Ex. 1107)</th>
</tr>
</thead>
<tbody>
<tr>
<td>21. The method of claim 17, wherein</td>
<td>See above discussion of ‘585 patent, claim 17.</td>
</tr>
<tr>
<td>said center frequency and said sampling frequency are functions of said intermediate frequency</td>
<td>See above discussion of ‘585 patent, claim 6.</td>
</tr>
<tr>
<td></td>
<td>see also Ex. 1113, Hashemi’s Dec., ¶¶121, 122, and 127.</td>
</tr>
</tbody>
</table>


1. Motivation to Combine VDP, Ishikawa and Tsividis

Theory, design, and implementation of filter circuits have been well known for several decades. Tsividis provides an overview of integrated continuous-time filter design. (See, e.g., Ex. 1108, Tsividis, title.) The Gm-C filter was a well type of integrated continuous-time filter. (Id. at p. 167, “Gm-C filters were employed commercially quite early [16], [17] using bipolar technology.”) (Ex. 1113, Hashemi’s Dec., ¶¶128-133).
Electrical filters can be realized using only passive components or using a combination of passive and active components. (Id.) Passive-only realization of band-pass filters requires using inductors or resonators – both of which require a significant footprint and are too lossy to be practical for integrated circuit monolithic realization. (Id.) Active filters are more compact and suitable for monolithic integrated circuit realization. (Id.) The common active filter realizations are Gm-C (also known as transconductance capacitor) and switched capacitor; both have been used heavily in communication receivers over the past. (Id.)

It is completely obvious and somewhat common practice for a POSTIA to use a Gm-C band-pass filter for anti-aliasing. (Id.) Therefore, a POSITA would be motivated to use concepts from Tsividis with VDP in view of Ishikawa for monolithic integrated circuit realization. (Id.) The motivation to combine VDP and Ishikawa is described in section VI.A above.

2. Combining VDP, Ishikawa and Tsividis

Tsividis describes the application of continuous time (CT) filter design for anti-alias filters in television receivers:

CT filters can also be used for anti-aliasing purposes, before signals are sampled in order to be A/D converted (or in order to be processed by an analog sampled-data signal processor). They can also be used
for smoothing purposes at the output of DAC's (and sampled-data analog processors). Such applications include anti-aliasing for digital audio [11], as well as for digital TV [12] and HDTV [13]. (Ex. 1108, Tsividis, p. 166.) In particular, the use of a transconductance (gmC) filter function for anti-aliasing filters in TV receivers was well known:

A transconductor can be developed by sensing the current of a resistor, across which the input voltage is precisely applied with the help of accurate buffers implemented with feedback [13], [14], [17]. This produces a linear transconductor which cannot, however, itself by tuned. To provide tunability, one can pass the current through a variable current multiplier [13], [14], [17]. Unless this is done carefully, the latter can add distortion and noise. By careful design, though, impressive results can be produced; a recent filter chip [13] achieves wide-band operation (8 MHz) with a 10-b equivalent linearity, for 5 Vpp signals, thus attaining performance compatible with HDTV anti-aliasing requirements for the MUSE system. (Id. at p. 171.) Depending on the signal to sampled, anti-alias filters may be implemented as a low-pass filter or a bandpass filter. (Ex. 1113, Hashemi’s Dec., ¶133). In figure 5 below, Tsividis illustrates a Gm-C second-order filter circuit for low-pass and bandpass (Ex. 1108, Tsividis, p. 168. “An example of a Gm-C second-order filter is shown in Fig. 5 [15]. It provides low-pass and bandpass outputs for the same input.”):
8. The receiver of claim 1, wherein said anti-aliasing filter comprises a transconductance (gmC) filter function.

See above discussion of ‘585 patent, claim 1.

See, e.g., Ex. 1108, Tsividis, p. 166 (“CT filters can also be used for anti-aliasing purposes, before signals are sampled in order to be A/D converted (or in order to be processed by an analog sampled-data signal processor). They can also be used for smoothing purposes at the output of DAC's (and sampled-data analog processors). Such applications include anti-aliasing for digital audio [11], as well as for digital TV [12] and HDTV [13]. “);

Ex. 1108, Tsividis, p. 171 (“A transconductor can be developed by sensing the current of a resistor, across which the input voltage is precisely applied with the help of accurate buffers implemented with feedback [13], [14], [17]. This produces a linear transconductor which cannot, however, itself be tuned. To provide tunability, one can pass the current through a variable current multiplier [13], [14], [17]. Unless this is done carefully, the latter can add distortion and noise. By careful design, though, impressive results can be produced; a recent filter chip [13] achieves wide-band operation (8 MHz)
with a 10-b equivalent linearity, for 5 Vpp signals, thus attaining performance compatible with HDTV anti-aliasing requirements for the MUSE system.”;

Ex. 1108, Tsividis, p. 168 (“An example of a Gm-C second-order filter is shown in Fig. 5 [15]. It provides low-pass and bandpass outputs for the same input.”);

Ex. 1108, Tsividis, Fig. 5 (showing a Gm-C filter).

see also Ex. 1113, Hashemi’s Dec., ¶¶129-134.)


1. Motivation to Combine VDP, Ishikawa and Greenberg

Greenberg is a “circuit architecture suitable for use in a television receiver.” (See, e.g., Ex. 1110, Greenberg, Abstract.) Therefore, a POSITA would be motivated to use concepts from Greenberg with the television receiver of VDP in view of Ishikawa as described in VI.A above. (Ex. 1113, Hashemi’s Dec., ¶¶135-141.) The motivation to combine VDP and Ishikawa is described in section VI.A above.

It would have been obvious to incorporate the Greenberg filter circuit in order to add the flexibility of being able to reloaded filter coefficients without having to change hardware. (See, e.g., Ex. 1110, Greenberg, Abstract “The apparatus features a filter circuit architecture which can be configured under programmed control so as to partition groups of its filter sections to form IIR filters
and FIR filters. The filter architecture is suitable for use in multi-circuit configurations and can be used with clustering algorithms to increase the efficiency and optimize the use of the available circuit architecture,” emphasis added; see also, Ex. 1113, Hashemi’s Dec., ¶¶135-141.).

2. **Combining VDP, Ishikawa and Greenberg**

   It would have been obvious to constitute the FIR filters in a manner that enables retrieval from memory based on transmission mode. (Id.) For example, Greenberg teaches the storage and retrieval FIR coefficients by a DSP. (See, e.g. Ex. 1110, Greenberg, 4:39-42 “Filter circuit 200 is periodically reloaded with coefficients calculated by processor 25 which can be a microprocessor or digital signal processor (DSP).”) Greenberg, Figure 3, below shows Digital Filter Chip (FIR and IIR) 200, which is operably connected to the DSP 25, which comprises ROM and RAM.
Greenberg’s DSP 25 is suitable for use in a television receiver which effectively performs a ghost or echo cancellation (See Ex. 1110, Greenberg, Abstract), such as the receiver in the ‘585 patent. (See Ex. 1101, ‘585 patent, 5:28-40 “DSP 64 can also implement other filter functions such as ghost cancellation for reducing the interference of the input signal….Furthermore, additional filter functions, such as an equalizer for echo cancellation (multipath), can also be implemented in DSP 64;” Ex. 1113, Hashemi’s Dec., ¶138.)

Furthermore, Greenberg teaches programmable FIR filters (See, e.g., Ex. 1110, Greenberg, Abstract) with coefficients that can be loaded from a DSP with memory. (Ex. 1110 at 4:39-42 and 4:60-5:2; Ex. 1113, Hashemi’s Dec., ¶139.).
The address provided at A<2:0> by Greenberg’s processor 25 indexes the memory to retrieve one of said plurality of finite impulse response filters, e.g. by way of the coefficient data. (See, e.g., Ex. 1110 9:12-18 “Register 902 holds eight bits of coefficient data provided to each of the filter stages 800 as "coef in" on bus 915. Coefficient data is made available to interface circuit 900 at its DATA<7:0> port, from processor 25. The address provided at A<2:0> by the processor 25, selects register 902 as the destination for the coefficient data.”; Ex. 1113, Hashemi’s Dec., ¶140.)

<table>
<thead>
<tr>
<th>'585 Patent – Claim 11</th>
<th>VDP (Ex. 1104), Ishikawa (Ex. 1105) and Greenberg (Ex. 1110)</th>
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<tbody>
<tr>
<td>11. The receiver of claim 10, wherein said plurality of finite impulse response filters are stored in a memory, and said signal processor indexes said memory to retrieve one of said plurality of finite impulse response filters.</td>
<td>See above discussion of ’585 patent, claim 10.</td>
</tr>
<tr>
<td></td>
<td>See Ex. 1110, Greenberg, Abstract (&quot;A circuit architecture suitable for use in a television receiver which effectively performs a ghost or echo cancellation procedure on post echo components and pre echo components occurring within the transmission channel. The apparatus features a filter circuit architecture which can be configured under programmed control so as to partition groups of its filter sections to form IIR filters and FIR filters.&quot;); Greenberg, 4:39-42 (&quot;Filter circuit 200 is periodically reloaded with coefficients calculated by processor 25 which can be a microprocessor or digital signal processor (DSP). The algorithms used to derived the coefficients are stored in memory which can be part of the processor 25. The processor also provides control words which configure and implement the functions of the filter circuit 200 as</td>
</tr>
</tbody>
</table>
described in more detail below.”); Greenberg, 4:60-5:2 (“Each filter section comprises a section configuration register 600, an input select circuit 700 and a filter stage 800 comprising a plurality of taps (e.g. twenty). An interface circuit 900 receives data from processor 25 which includes coefficient data and configuration data, and provides control words and coefficients to the rest of the filter circuit 200. Final adder circuit 400 provides circuit input, output, summation and scaling functions for the filter circuit 200, under the control of control words provided by interface circuit 900.”); and Greenberg, 9:12-18 (“Register 902 holds eight bits of coefficient data provided to each of the filter stages 800 as "coef in" on bus 915. Coefficient data is made available to interface circuit 900 at its DATA<7:0> port, from processor 25. The address provided at A<2:0> by the processor 25, selects register 902 as the destination for the coefficient data.”).

See also, e.g., Ex. 1110, Greenberg, Fig. 3 (Showing Digital Filter Chip (FIR and IIR) 200, which is operably connected to the DSP 25 with ROM and RAM);

See also Ex. 1113, Hashemi’s Dec., ¶¶135-141.

VII. CONCLUSION

The combination of VDP and Ishikawa renders claims 1, 2, 4, 5, 10 and 12-20 obvious. The addition of Malkemes to the combination of VDP and Ishikawa renders claim 3 obvious. The addition of Balaban to the combination of VDP and Ishikawa renders claims 6, 7, 9 and 21 obvious. The addition of Tsividis to the combination of VDP and Ishikawa renders claim 8 obvious. The addition of
Greenberg to the combination of VDP and Ishikawa renders claim 11 obvious.

Petitioner therefore requests institution of an *inter partes* review to cancel claims 1–21 of the ’585 patent.

Dated: January 28, 2015

Respectfully submitted,

/Thomas J. Wimbiscus/
Thomas J. Wimbiscus
Registration No. 36,059
McAndrews, Held & Malloy, Ltd.
500 West Madison Street, 34th Floor
Chicago, Illinois 60661
Office: (312) 775-8000
Fax: (312) 775-8100
twimbiscus@mcandrews-ip.com

*Lead Counsel for Patent Owner*
CERTIFICATE OF SERVICE

I hereby certify that, on January 28, 2015, a true and correct copy of the following materials:

- PETITION FOR INTER PARTES REVIEW OF 7,075,585 UNDER 35 U.S.C. § 312 AND 37 C.F.R. § 42.104
- Exhibits 1101–1136
- Table of Exhibits
- Fee Authorization
- Power of Attorney

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<table>
<thead>
<tr>
<th>Law Office of Andrei D. Popovici, P.C.</th>
<th>Genevieve Vose Wallace</th>
</tr>
</thead>
<tbody>
<tr>
<td>ATTN: Andrei Popovici</td>
<td>Floyd G. Short</td>
</tr>
<tr>
<td>4030 Moorpark Ave., Suite 108</td>
<td>Parker C. Folse</td>
</tr>
<tr>
<td>San Jose, CA 95117</td>
<td>Susman Godfrey LLP</td>
</tr>
<tr>
<td></td>
<td>1201 Third Avenue, Suite 3800</td>
</tr>
<tr>
<td></td>
<td>Seattle, Washington 98101</td>
</tr>
</tbody>
</table>

MCANDREWS HELD & MALLOY

Telephone: 312-775-8000
Facsimile: 312-775-8100

CUSTOMER NUMBER: 23446
Date: January 28, 2015

/Thomas J. Wimbiscus/
Thomas J. Wimbiscus
Registration No. 36,059

Date: January 28, 2015

/Thomas J. Wimbiscus/